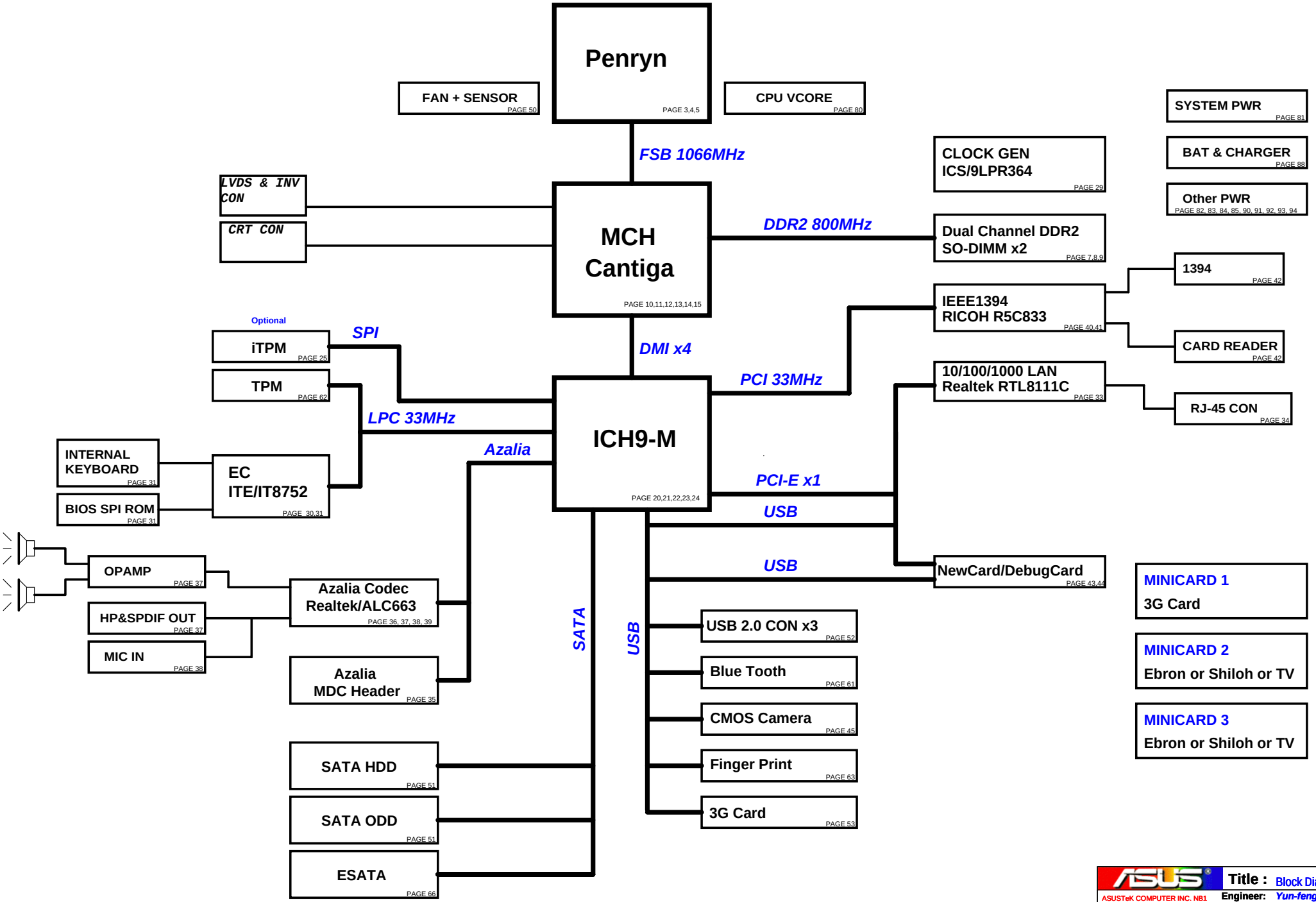
N50A/N51A Montevina Block Diagram



ASUSTeK COMPUTER INC. NB1	Title : Block Diagram	
	Engineer: Yun-feng_yan	
Size: Custom	Project Name: N50A/N51A	Rev: 1.0
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90	POWER_DETECT
91	POWER_LOAD SWITCH
92	POWER_PROTECT
93	POWER_SIGNAL
94	POWER_FLOWCHART

GPIO33 Internal Pull High, Go Low= Flash
Descriptor Security will be overriden

ICH9-M GPIO	Use As	Signal Name	Power
GPIO 00	GPI	PMSYNC#(programmed as GPO)	+3VS
GPIO 01	GPI	DOCKING_DET# EXT PU	+3VS
GPIO [2:5]	GPI	PCI_INT[E:H]# EXT PU	+5VS
GPIO 06	GPI	- EXT PU	+3VS
GPIO 07	GPI	- EXT PU	+3VS
GPIO 08	GPI	EXT_SMI# EXT PU	+3VSUS
GPIO 09	Native	WOL_EN	+3VSUS
GPIO 10	GPI	RTLAN_DSM# EXT PU	+3VSUS
GPIO 11	Native	EXT_SCI#(Programmed as GPI	+3VSUS
GPIO 12	GPO	-	+3VSUS
GPIO 13	GPI	CB_SD#(Programmed as GPO)	+3VSUS
GPIO 14	GPI	AC_PRESENT EXT PD	+3VSUS
GPIO 15	Native	STP_PCI#	+3VSUS
GPIO 16	Native	PM_DPRSLPVR INT PD*	+3VS
GPIO 17	GPI	WLAN_LED(Programmed as GPO	+3VS
GPIO 18	GPO	-	+3VS
GPIO 19	GPI	- EXT PU	+3VS
GPIO 20	GPO	- INT PD*	+3VS
GPIO 21	GPI	- EXT PU	+3VS
GPIO 22	GPI	BT_DET# EXT PU	+3VS
GPIO 23	Native	ICH_LDRQ1# INT PU	+3VS
GPIO 24	GPO	WLAN_ON	+3VSUS
GPIO 25	Native	STP_CPU#	+3VSUS
GPIO 26	Native	PM_S4_STATE#	+3VSUS
GPIO 27	GPO	BT_ON	+3VSUS
GPIO 28	GPO	BT_LED	+3VSUS
GPIO 29	Native	NEWCARD_OC#	+3VSUS
GPIO 30	Native	USB_OC3467#	+3VSUS
GPIO 31	Native	USB_OC3467#	+3VSUS
GPIO 32	GPO	PM_CLKRUN#	+3VS
GPIO 33	GPO	- INT PU*	+3VS
GPIO 34	GPO	-	+3VS
GPIO 35	GPO	-	+3VS
GPIO 36	GPI	- EXT PU	+3VS
GPIO 37	GPI	PCB_ID0	+3VS
GPIO 38	GPI	PCB_ID1	+3VS
GPIO 39	GPI	PCB_ID2	+3VS
GPIO 40	Native	USB_OC01#	+3VSUS
GPIO 41	Native	USB_OC2#	+3VSUS
GPIO 42	Native	USB_OC3467#	+3VSUS
GPIO 43	Native	USB_OC3467#	+3VSUS
GPIO 44	Native	CLK_DEC#	+3VSUS
GPIO 45	Native	CLK_ACC	+3VSUS
GPIO 46	Native	WLAN_ON	+3VSUS
GPIO 47	Native	UNDOCKING#	+3VSUS
GPIO 48	GPI	EMAIL_LED# EXT PU	+3VS
GPIO 49	GPO	GPU_RST# INT PU*	**+3VS**
GPIO 50	Native	PCI_REQ#1	+5VS
GPIO 51	Native	PCI_GNT#1 INT PU*	+3VS
GPIO 52	Native	PCI_REQ#2	+5VS
GPIO 53	Native	PCI_GNT#2 INT PU*	+3VS
GPIO 54	Native	PCI_REQ#3	+5VS
GPIO 55	Native	PCI_GNT#3 INT PU*	+3VS
GPIO 56	GPI	- EXT PU	+3VSUS
GPIO 57	GPI	- EXT PU	+3VSUS
GPIO 58	GPI	SPI_CS#1 INT PU*	+3VSUS
GPIO 59	Native	USB_OC0#	+3VSUS
GPIO 60	Native	RTLAN_DSM_EN	+3VSUS

EC GPIO	Use As	Signal Name	Power
GPA0	GPO	PWR_LED_UP#	
GPA1	GPO	CHG_LED_UP#	
GPA2	GPO	BATSEL_3S#	
GPA3	-	-	
GPA4	GPO	LCD_BL_PWM	
GPA5	GPO	FAN0_PWM	
GPA6	GPO	BAT1_CNT1#	
GPA7	GPO	BAT2_CNT1#	
GPB0	GPO	CHG_EN#	
GPB1	GPO	PRECHG	
GPB2	GPI	DISTP#	
GPB3	ALT	SMB0_CLK	
GPB4	ALT	SMB0_DAT	
GPB5	OD	A20GATE	
GPB6	OD	RCIN#	
GPB7	GPO	PM_RSMRST#	
GPC0	GPI	MARATHON#	
GPC1	ALT	SMB1_CLK	
GPC2	ALT	SMB1_DAT	
GPC3	GPO	PM_PWRBTN#	
GPC4	ALT	AC_IN_OC#	
GPC5	GPO	OP_SD#	
GPC6	ALT	BAT1_IN_OC#	
GPC7	GPO	3G_ON#	
GPD0	GPI	PWRLIMIT#	
GPD1	ALT	PM_S4_STATE#	
GPD2	ALT	BUF_PLT_RST#	
GPD3	OD	EXT_SCI#	
GPD4	OD	EXT_SMI#	
GPD5	GPO	LCD_BACKOFF#	
GPD6	ALT	FAN0_TACH	
GPD7	GPI	COLOREN#	
GPE0	GPO	VSUS_ON	
GPE1	GPO	SUSC_EC#	
GPE2	GPO	SUSB_EC1#	
GPE3	GPO	CPU_VRON	
GPE4	ALT	PWR_SW#	
GPE5	ALT	BAT2_IN_OC#	
GPE6	GPI	LID_SW#	
GPE7	GPO	PM_THERM#	
GPF0	GPI	BLUETOOTH#	
GPF1	GPI	WIRELESS#	
GPF2	ALT	PS2_CLK_5S_PD	
GPF3	ALT	PS2_DATA_5S_PD	
GPF4	ALT	TP_CLK	
GPF5	ALT	TP_DAT	
GPF6	GPO	THRO_CPU	
GPF7	GPO	PS_SHDN#	
GPG0	GPI	INSTANT_ON#	
GPG1	ALT	PM_SUSB#	
GPG2	GPO	BAT1_CNT2#	
-	-	-	
-	-	-	

EC GPIO	Use As	Signal Name	Power
-	-	-	
GPG6	GPO	BAT2_CNT2#	
-	-	-	
GPH0	OD	PM_CLKRUN#	
GPH1	ALT	-	
GPH2	ALT	-	
GPH3	GPO	BAT_LEARN	
GPH4	GPO	-	
GPH5	GPO	NUM_LED	
GPH6	GPO	CAP_LED	
-	-	-	
GPI0	GPI	-	
GPI1	GPI	SUS_PWRGD	
GPI2	GPI	ALL_SYSTEM_PWRGD	
GPI3	GPI	VRM_PWRGD	
GPI4	GPI	PWR_MON	
GPI5	GPI	PD_DET#	
GPI6	GPI	KB_ID0	
GPI7	GPI	KB_ID1	
GPJ0	GPO	EC_CLK_EN	
GPJ1	GPO	PM_PWROK	
GPJ2	GPI	UNDOCK#_PD	
GPJ3	-	-	
GPJ4	GPO	BL_DA	
GPJ5	GPO	FAN_DA	
GPK0	GPI	PM_SLP_M#	
GPK1	GPI	SUSPWR_ACK	
GPK2	GPI	PM_SUSC#	
GPK3	GPI	+3VM_PG	
GPK4	GPI	+1.05VM_+3VMCLK_PG	
GPK5	GPI	LAN_WOL_EN	
GPL0	GPI	AC_APR_UC#	
GPL1	GPI	-	
GPL2	GPO	-	
GPL3	GPO	LAN_RST#	
GPL4	GPO	CL_PWROK	
GPL5	GPO	EC_WLAN_PWR	
GPL6	GPO	SLP_M_ON	
GPL7	GPO	S4_STATE_ON	
GPK6	GPO	AC_PRESENT	
GPK7	GPI	PS_CPPE#	

INT PU*: PU or PD in special time

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ASUSTeK COMPUTER INC. NB1 Engineer: <OrgAddr1>

Title : Schematic Information

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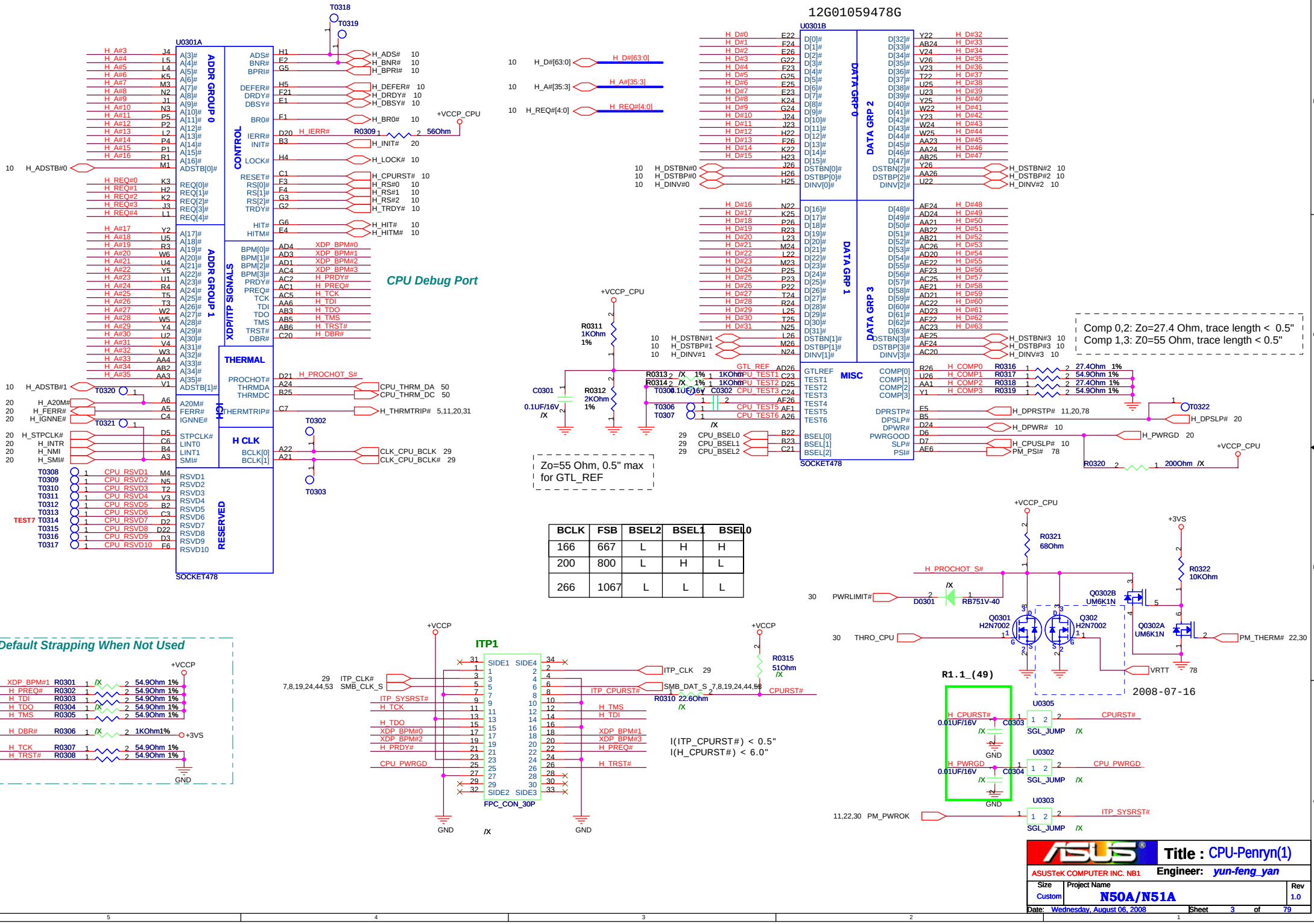
12G010059478G



CPU Debug Port

Zo=55 Ohm, 0.5" max for GTL_REF

Comp 0,2: Zo=27.4 Ohm, trace length < 0.5"
Comp 1,3: Z0=55 Ohm, trace length < 0.5"

BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	L	H	H
200	800	L	H	L
266	1067	L	L	L

ASUSTeK COMPUTER INC. NB1	Title : CPU-Penryn(1)			
	Engineer: yun-feng_yan			
Size: Custom	Project Name: N50A/N51A			Rev: 1.0
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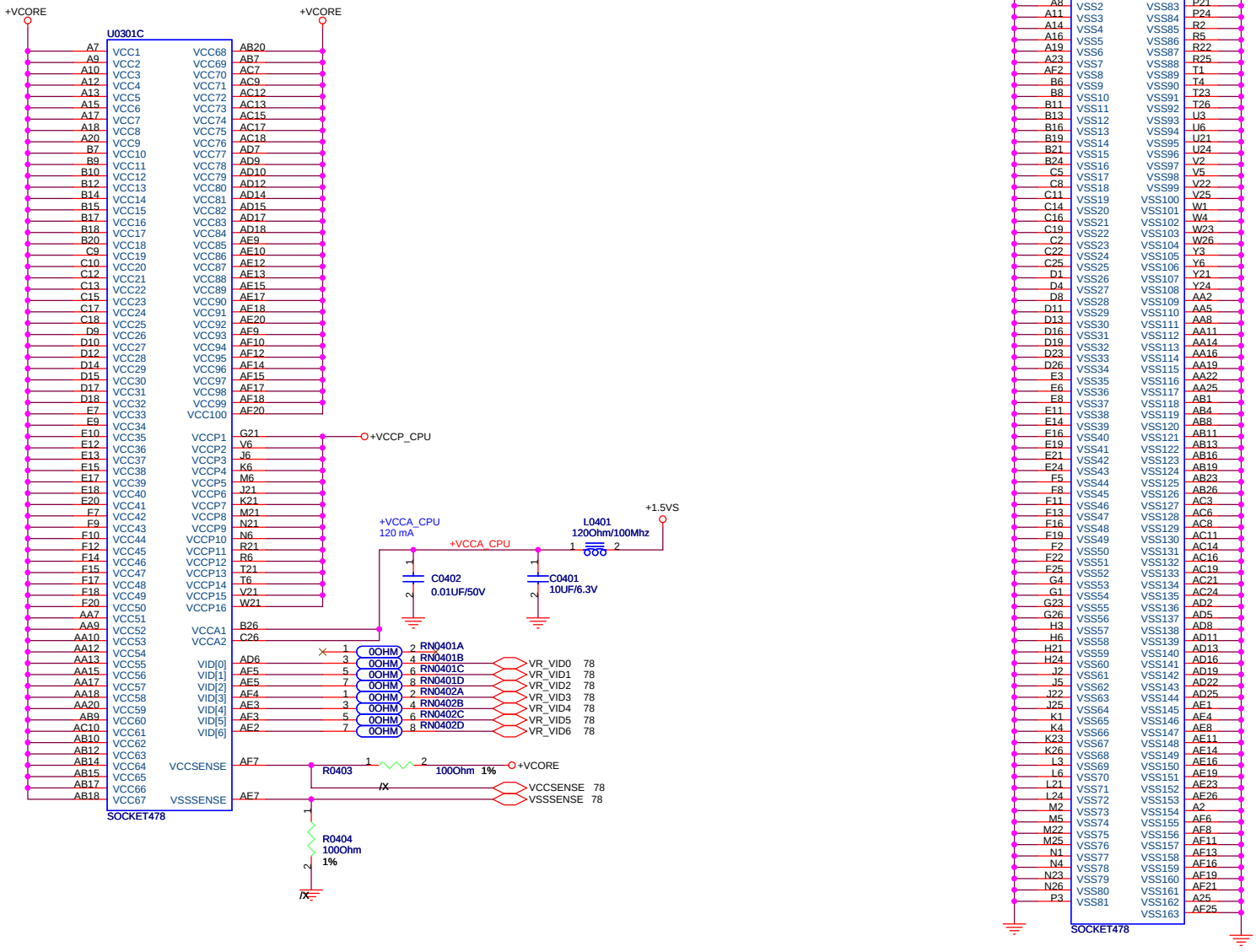

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ASUSTeK COMPUTER INC. NB1	Title : CPU-Penryn(2)	
	Engineer: yun-feng_yan	
Size: Custom	Project Name: N50A/N51A	Rev: 1.0
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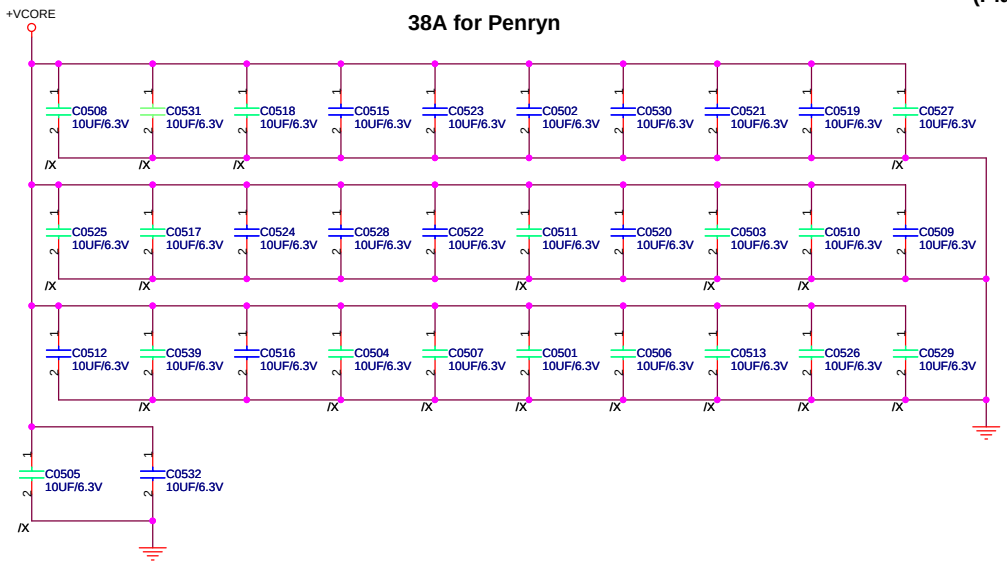
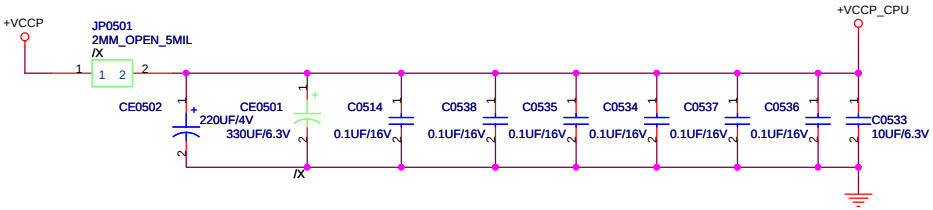
38A for Penryn



+VCCP Decoupling Capacitor (Place near CPU)

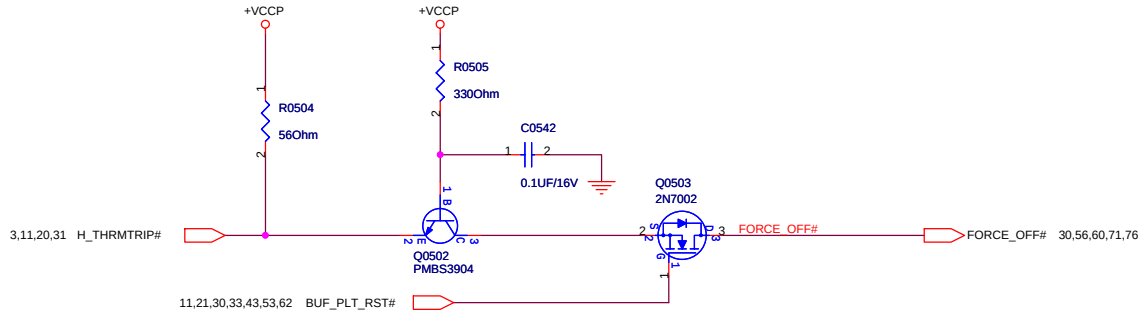
因爲CE0501與ME干涉,CE0501要移遠一點,而預留CE0502在原本CE0501位置



Decoupling guide from Intel

VCORE	22uF/10V r 10uF	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs
	150uF	* 1pcs ?
	10uF	* 1pcs ?

+VCORE Mid-Frequency Capacitor
*Intel: 22UF *32*
*F3S: 10UF *16*
*A7S: 10UF *10 ....11/17*
V1V: ?
+VCCP Decoupling Capacitor
*Intel: 270UF *1, 0.1UF *6*
*F3S: 100UF *1, 0.1UF *4*
V1V: ?



Thermal Trip signal (From CPU to ICH-9M and sequence)

Thermal trip control circit

ASUSTeK COMPUTER INC. NB1	Title : CPU CAPS	
	Engineer: yun-feng_yan	
Size: Custom	Project Name: N50A/N51A	Rev: 1.0
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ASUSTeK COMPUTER INC. NB1	Title :			
	Engineer: yun-feng_yan			
Size: A	Project Name: N50A/N51A			Rev: 1.0
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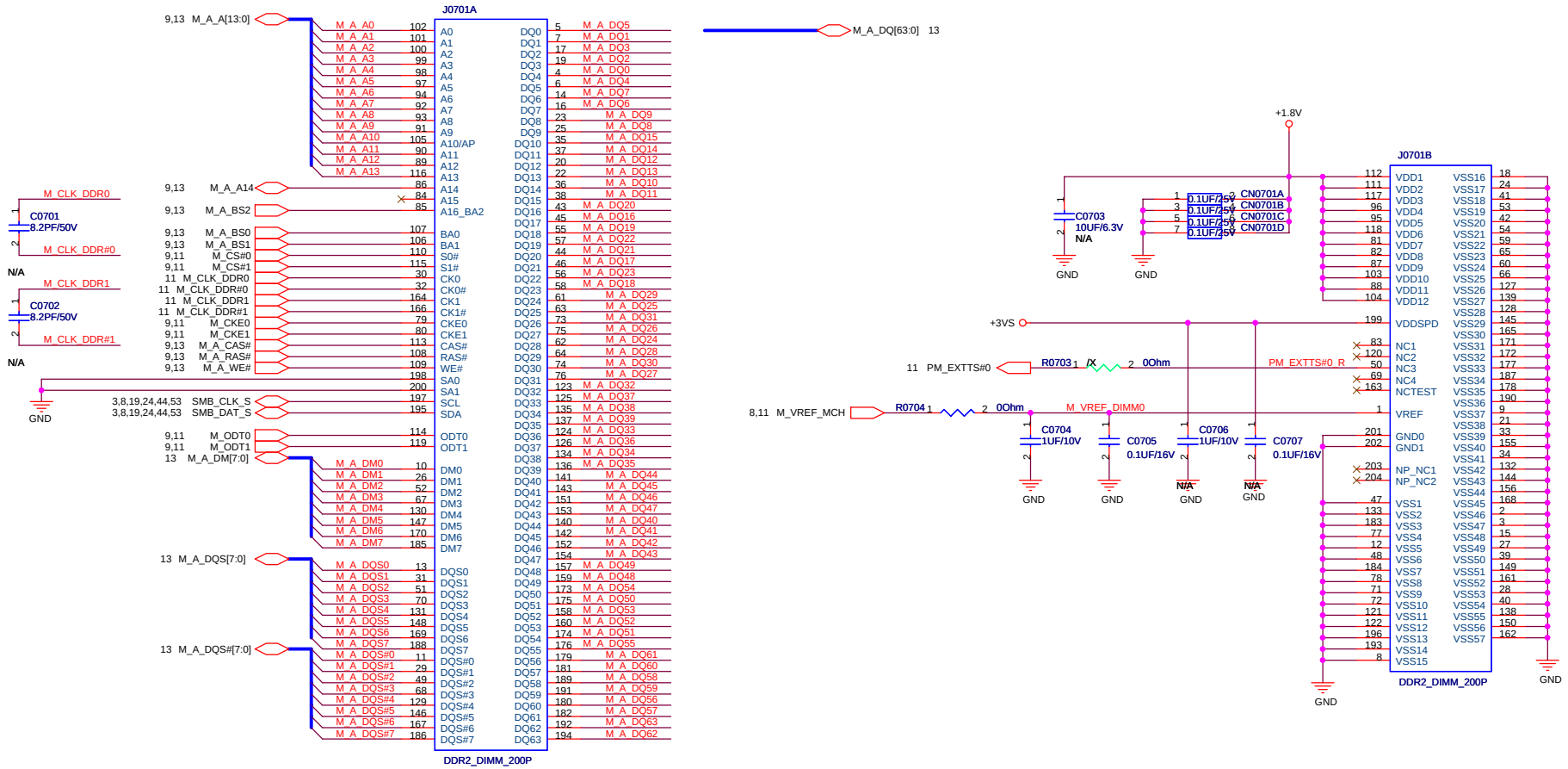
REV Type



ASUSTeK COMPUTER INC. NB1	Engineer: yun-feng_yan	
Size: Custom	Project Name: N50A/N51A	Rev: 1.0
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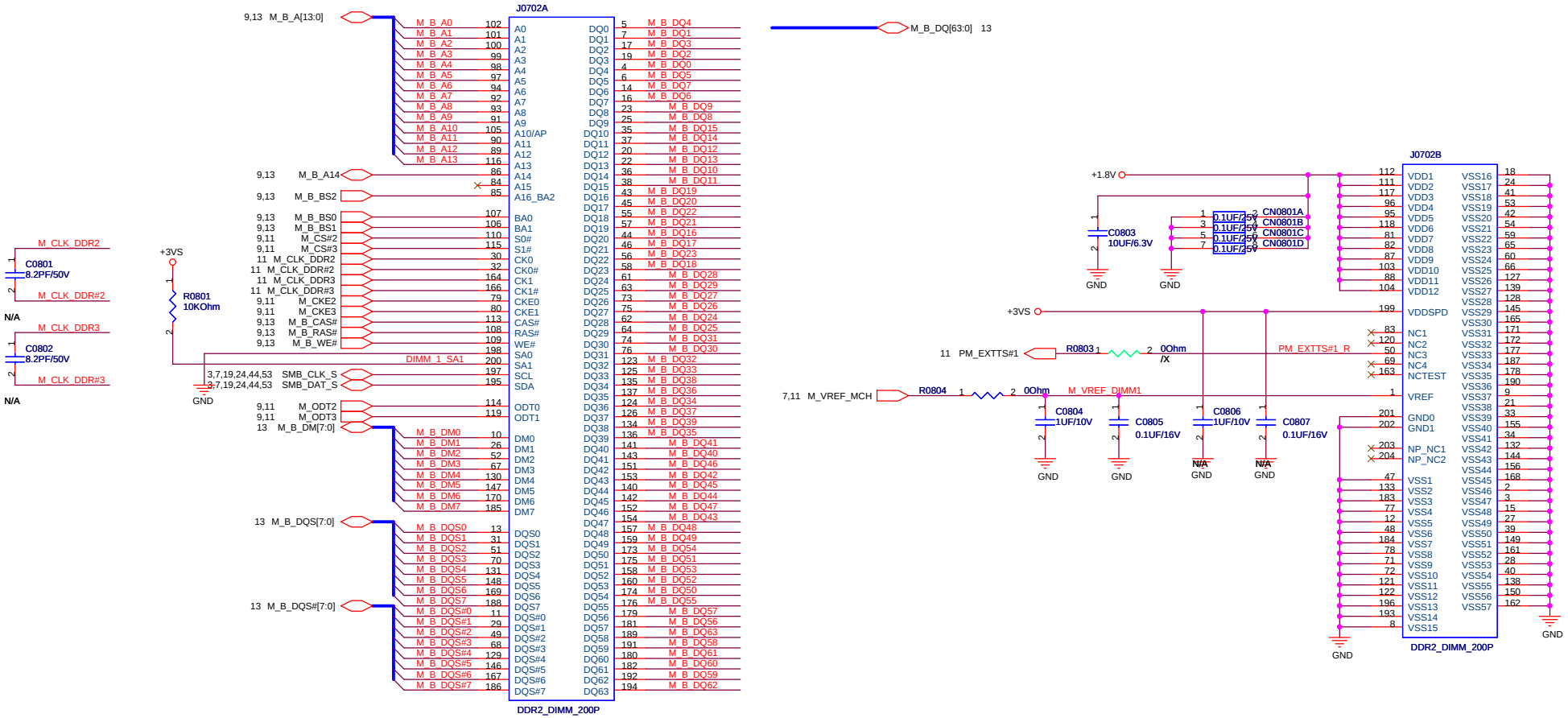
Title: DDR2 SO-DIMM_0

STD Type



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Title :DDR2 SO-DIMM_1

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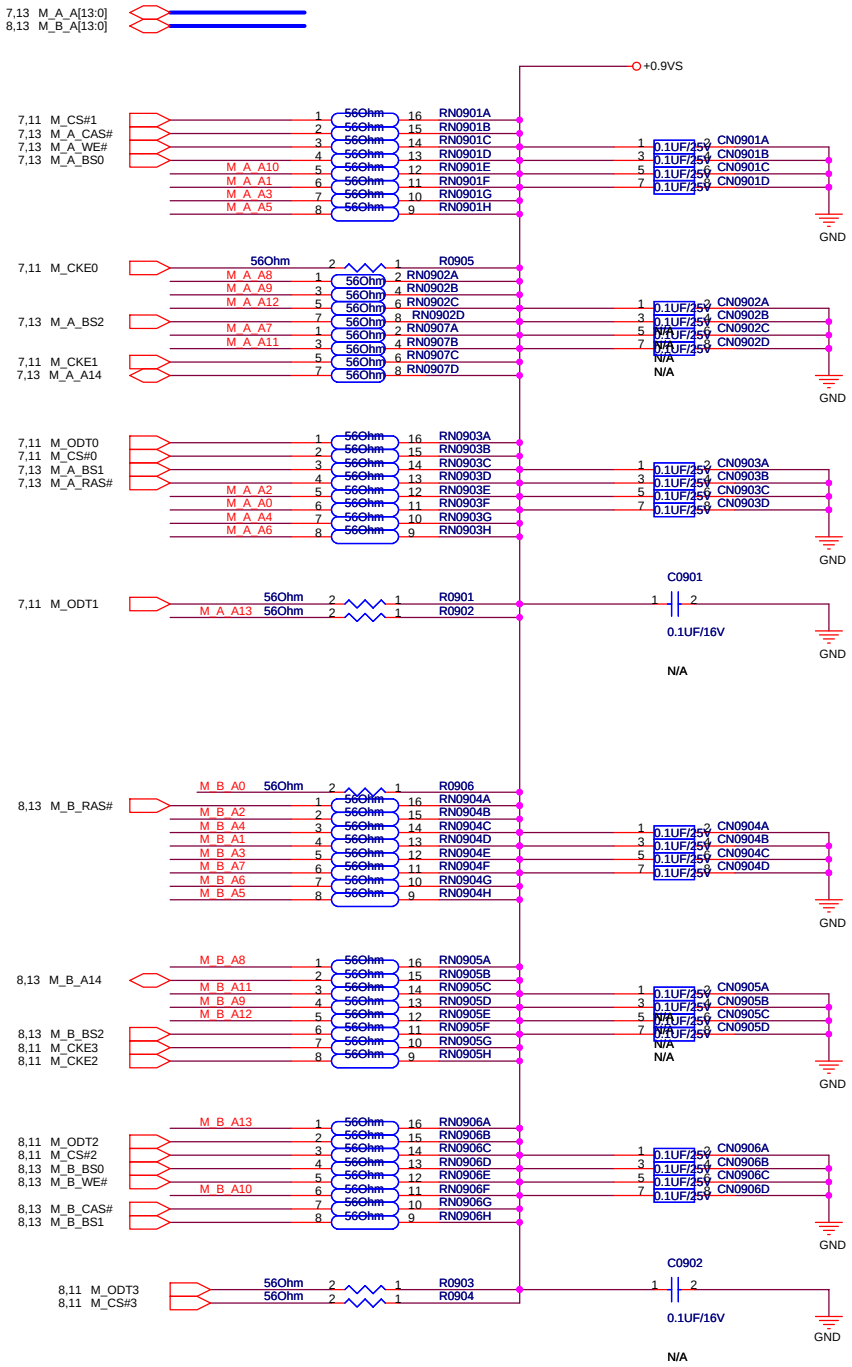

ASUSTeK COMPUTER INC. NB1	Title DDR2 termination	
	Engineer: yun-feng_yan	
Size: Custom	Project Name: N50A/N51A	Rev: 1.0
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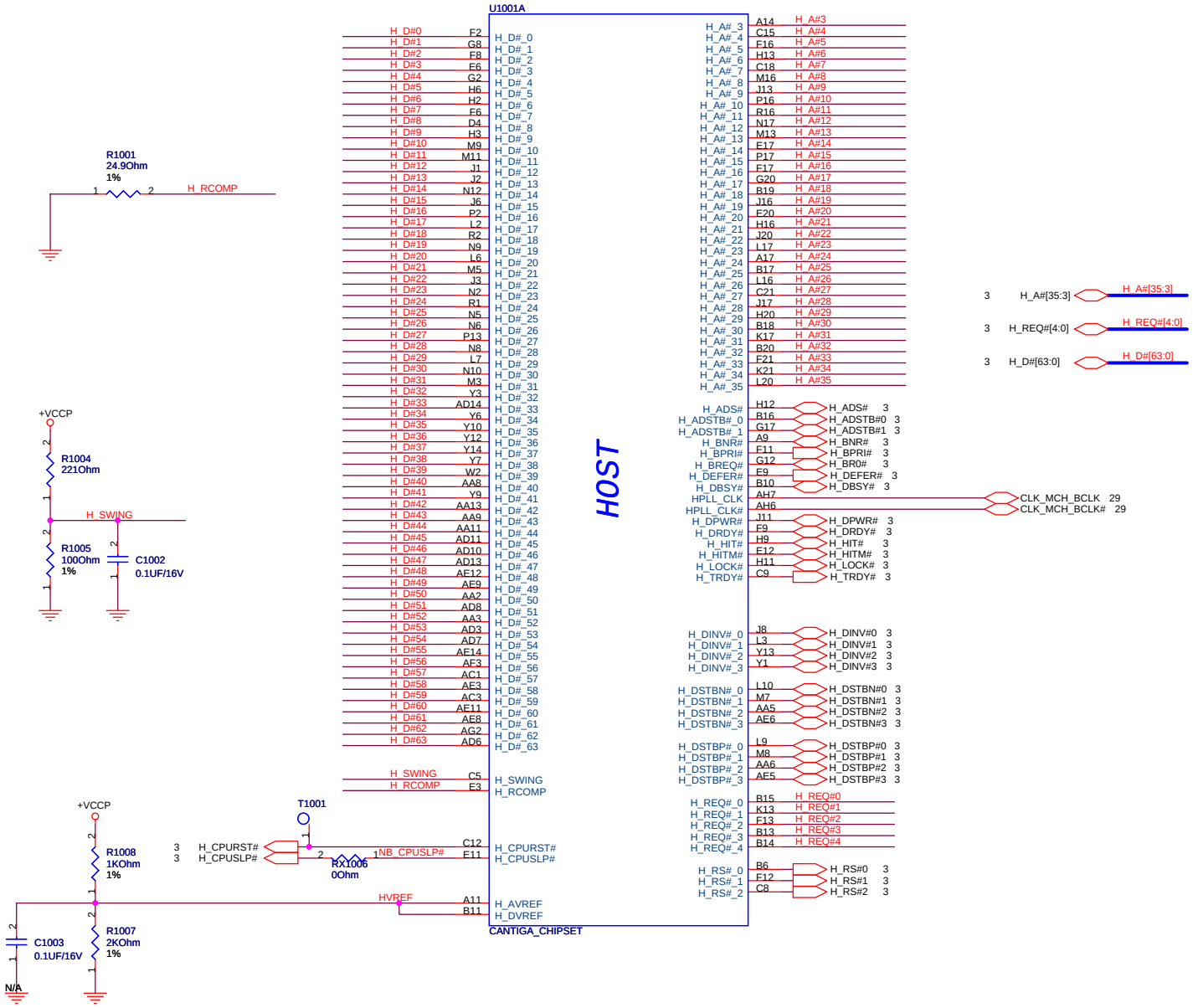

Cap 0.1uF within 100 mils from GMCH

ASUSTeK COMPUTER INC. NB1	Title : Cantiga -- CPU (1)	
	Engineer: yun-feng_yan	
Size: Custom	Project Name: N50A/N51A	Rev: 1.0
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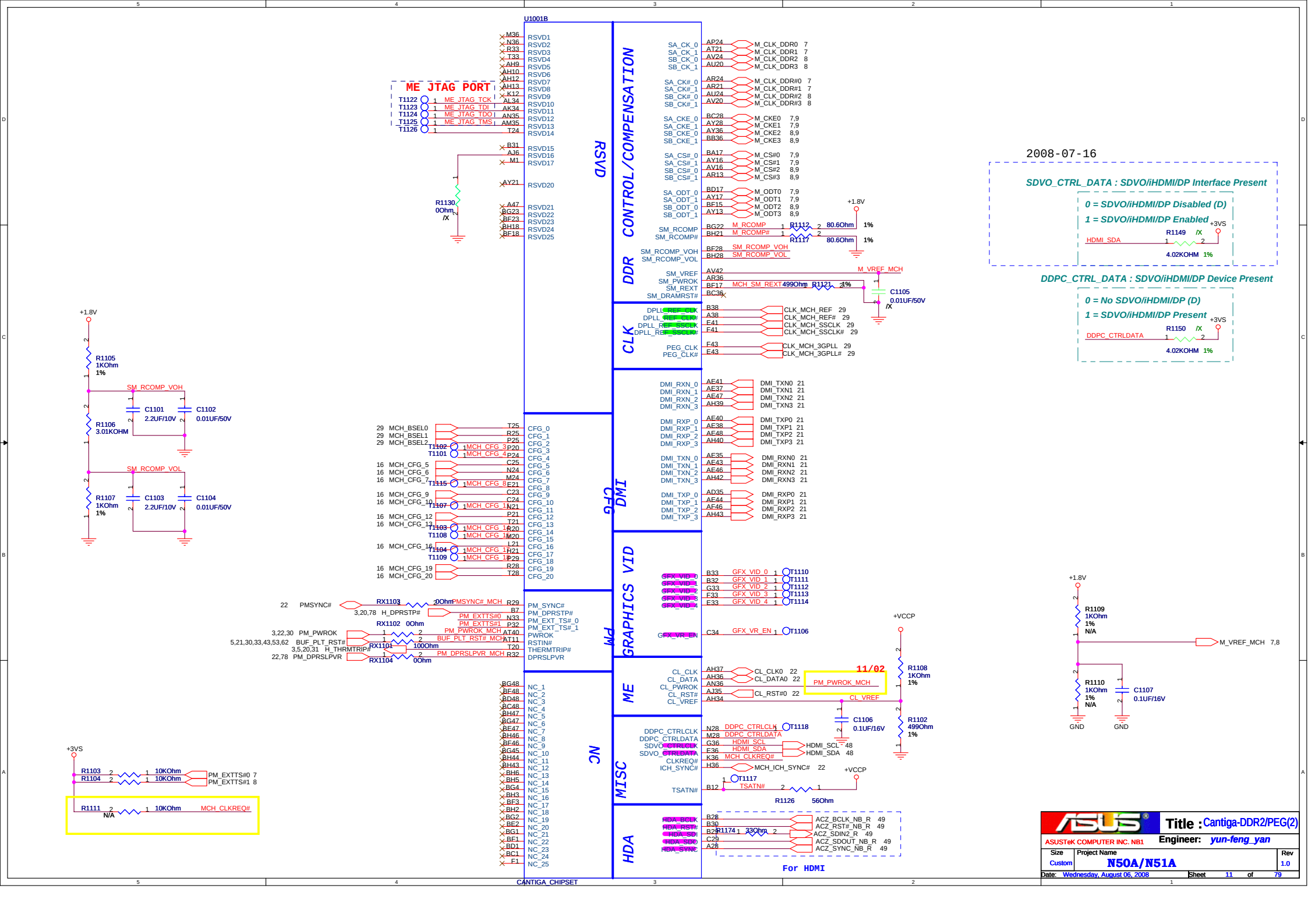
U1001B
RSVD
CONTROL/COMPENSATION
DDR
CLK
DMI
CFG
GRAPHICS VID
PM
ME
MISC
HDA
NC
CANTIGA_CHIPSET
ME JTAG PORT
ME_JTAG_TCK
ME_JTAG_TDI
ME_JTAG_TDO
ME_JTAG_TMS
R1130 0Ohm /X
SDVO_CTRL_DATA : SDVO/iHDMI/DP Interface Present
0 = SDVO/iHDMI/DP Disabled (D)
1 = SDVO/iHDMI/DP Enabled
R1149 /X 4.02KOHM 1%
DDPC_CTRL_DATA : SDVO/iHDMI/DP Device Present
0 = No SDVO/iHDMI/DP (D)
1 = SDVO/iHDMI/DP Present
R1150 /X 4.02KOHM 1%
2008-07-16
R1105 1KOhm 1%
R1106 3.01KOHM
R1107 1KOhm 1%
C1101 2.2UF/10V
C1102 0.01UF/50V
C1103 2.2UF/10V
C1104 0.01UF/50V
R1103 10KOhm
R1104 10KOhm
R1111 N/A 10KOhm
R1112 80.6Ohm 1%
R1117 80.6Ohm 1%
R1121 499Ohm 1%
C1105 0.01UF/50V /X
R1108 1KOhm 1%
R1109 1KOhm 1% N/A
R1110 1KOhm 1% N/A
C1107 0.1UF/16V
C1106 0.1UF/16V
R1102 499Ohm 1%
R1126 56Ohm
R1174 33Ohm
11/02
PM_PWROK_MCH
For HDMI
Title : Cantiga-DDR2/PEG(2)
Engineer: yun-feng_yan
ASUSTeK COMPUTER INC. NB1
Size Custom
Project Name N50A/N51A
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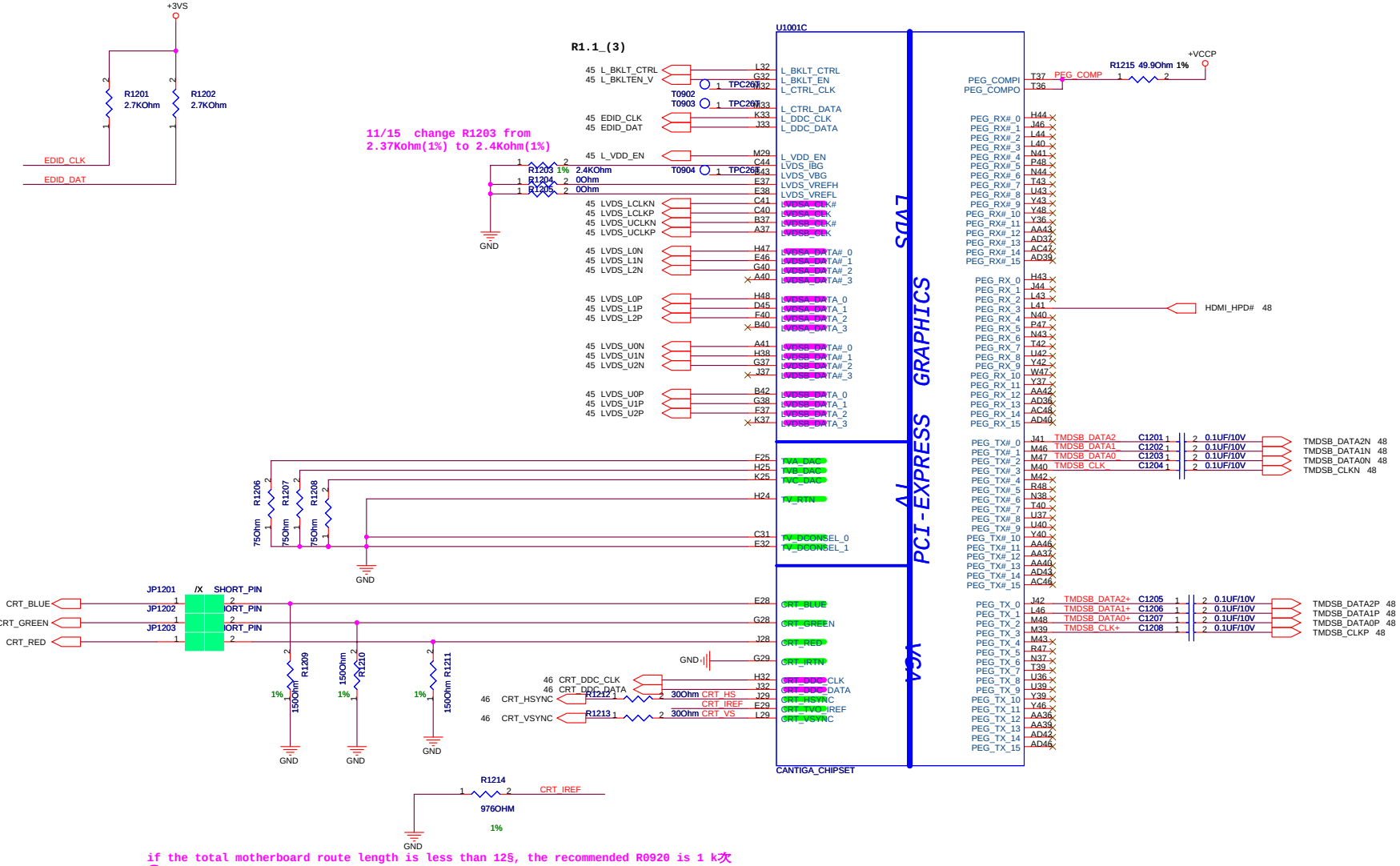

ASUSTeK COMPUTER INC. NB1	Title :	
	Engineer: <OrgAddr1>	
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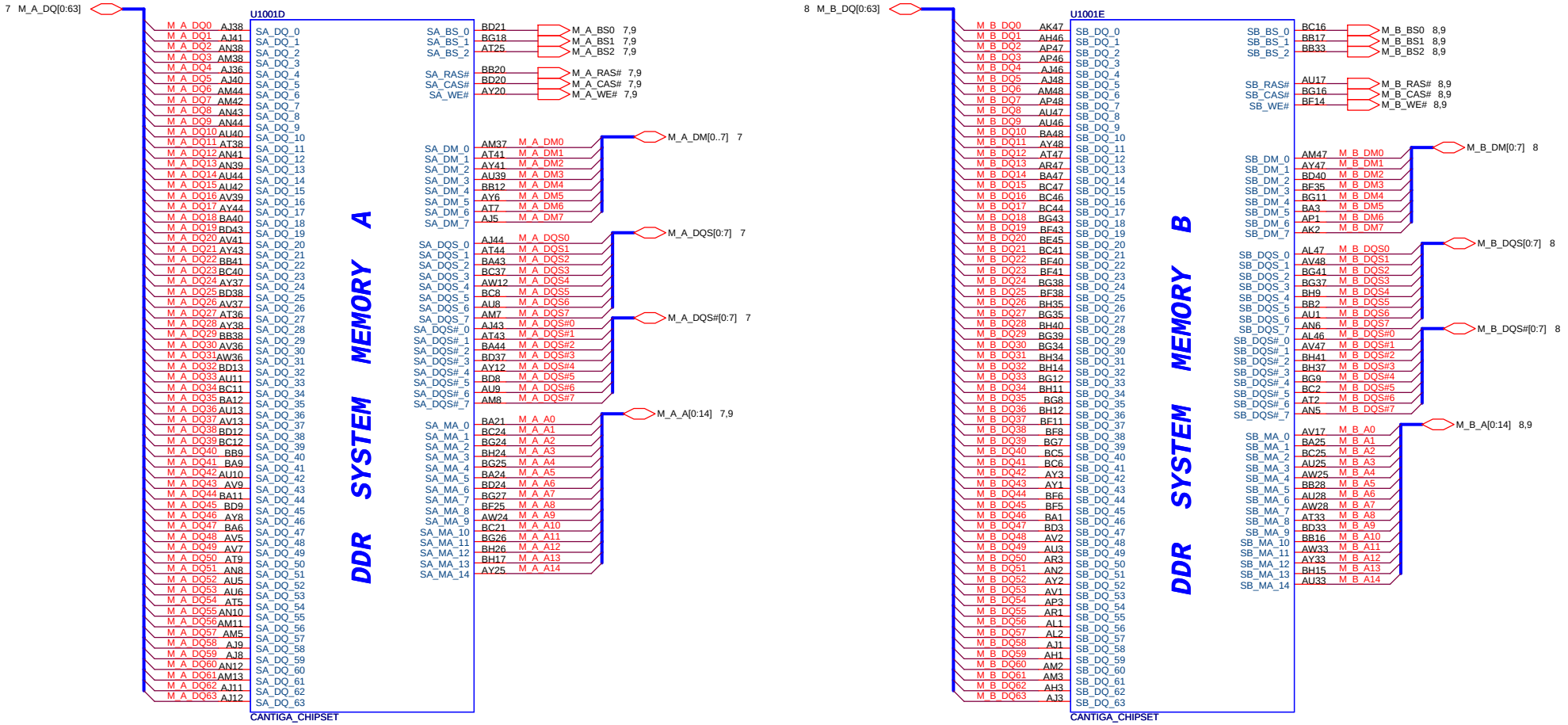

ASUSTeK COMPUTER INC. NB1	Title : Cantiga--DDR2 bus (3)	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50A/N51A	Rev: 1.0
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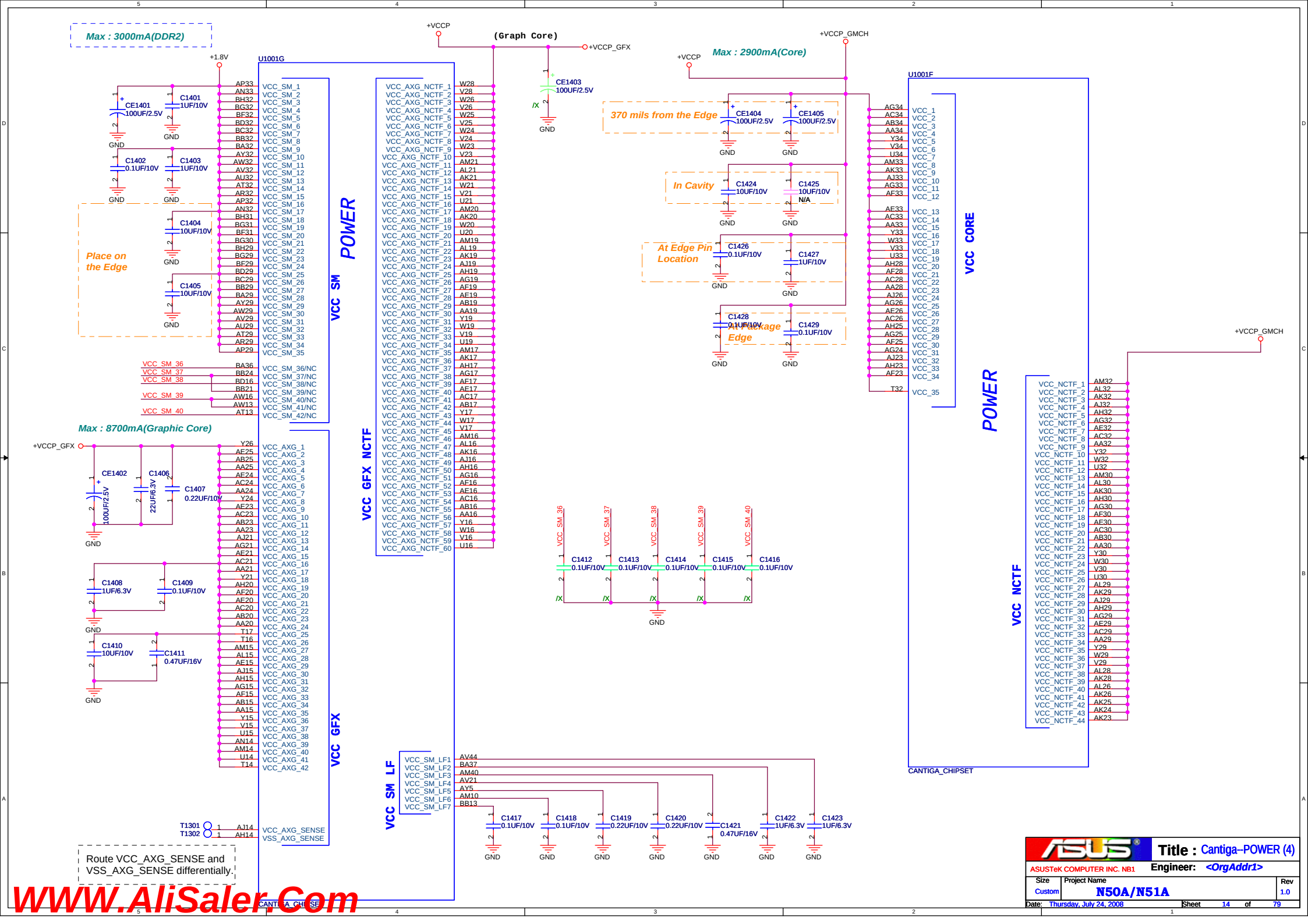
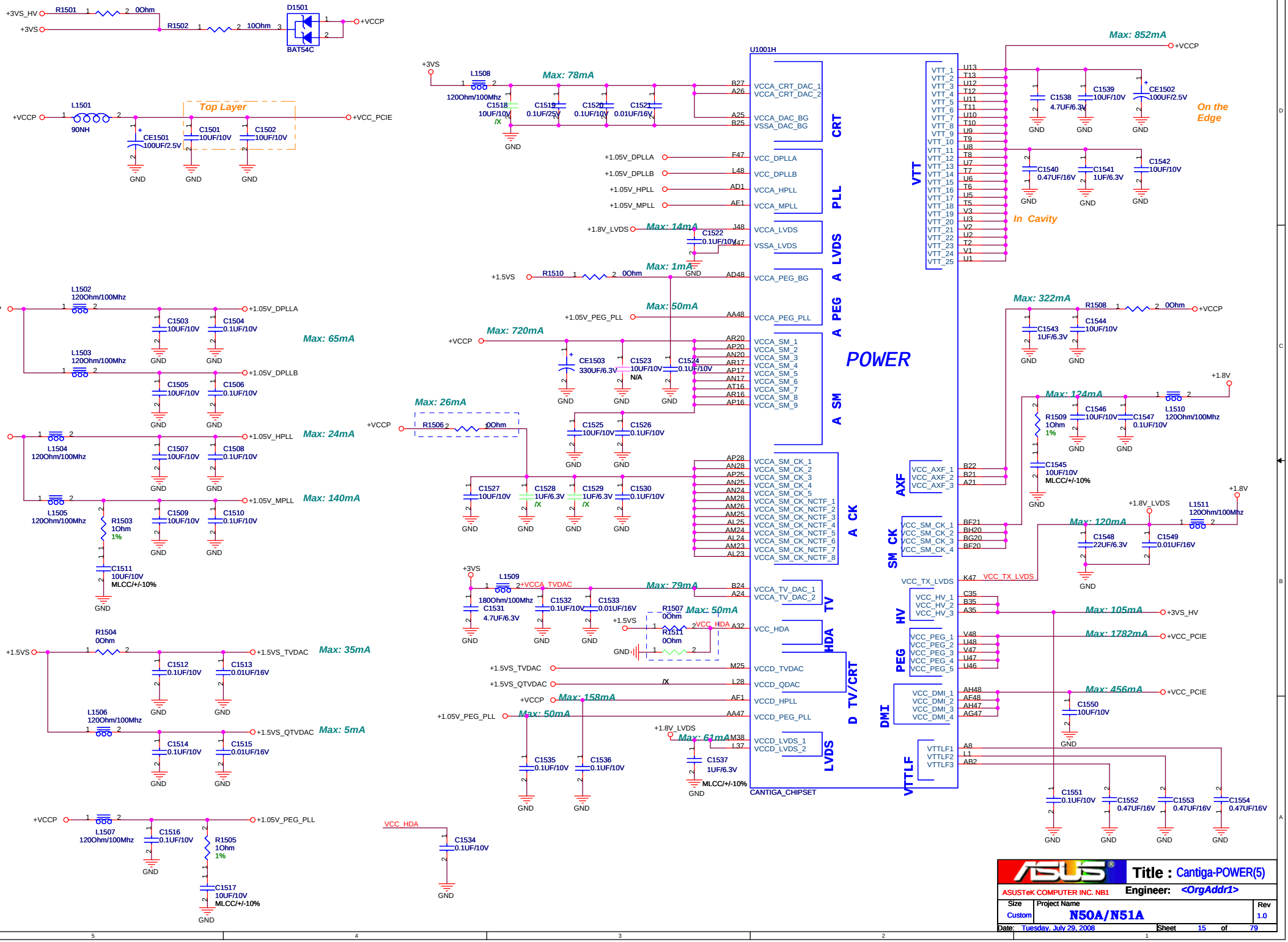
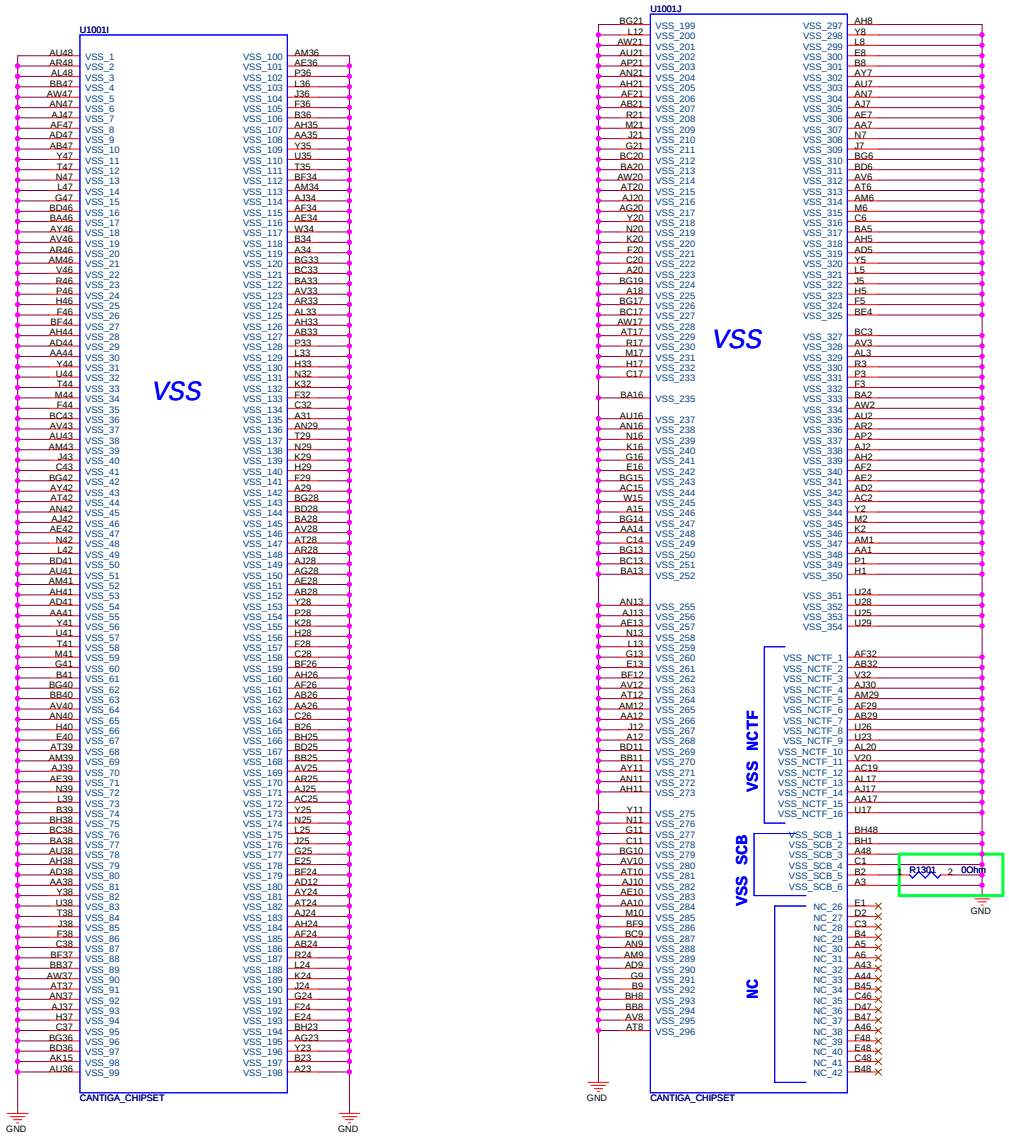
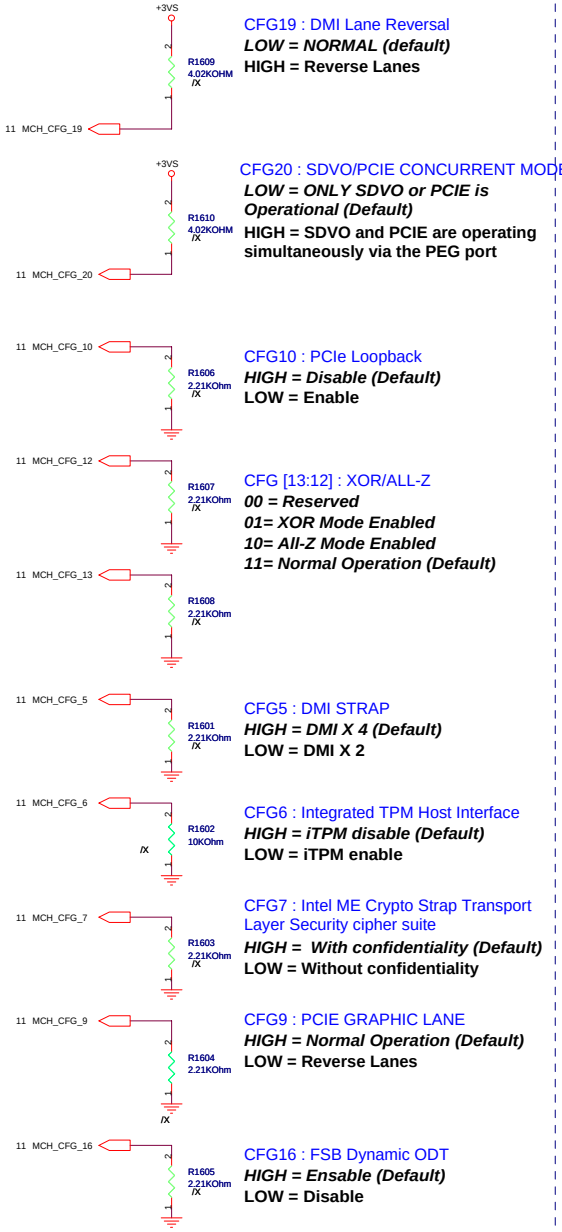

Max : 3000mA(DDR2)
+1.8V
U1001G
VCC_SM_1
VCC_SM_2
VCC_SM_3
VCC_SM_4
VCC_SM_5
VCC_SM_6
VCC_SM_7
VCC_SM_8
VCC_SM_9
VCC_SM_10
VCC_SM_11
VCC_SM_12
VCC_SM_13
VCC_SM_14
VCC_SM_15
VCC_SM_16
VCC_SM_17
VCC_SM_18
VCC_SM_19
VCC_SM_20
VCC_SM_21
VCC_SM_22
VCC_SM_23
VCC_SM_24
VCC_SM_25
VCC_SM_26
VCC_SM_27
VCC_SM_28
VCC_SM_29
VCC_SM_30
VCC_SM_31
VCC_SM_32
VCC_SM_33
VCC_SM_34
VCC_SM_35
CE1401 100UF/2.5V
C1401 1UF/10V
C1402 0.1UF/10V
C1403 1UF/10V
C1404 10UF/10V
C1405 10UF/10V
Place on the Edge
GND
VCC_SM_36
VCC_SM_37
VCC_SM_38
VCC_SM_39
VCC_SM_40
BA36
BB24
BD16
BB21
AW16
AW13
AT13
VCC_SM_36/NC
VCC_SM_37/NC
VCC_SM_38/NC
VCC_SM_39/NC
VCC_SM_40/NC
VCC_SM_41/NC
VCC_SM_42/NC
VCC SM
POWER
Max : 8700mA(Graphic Core)
+VCCP_GFX
CE1402 100UF/2.5V
C1406 22UF/6.3V
C1407 0.22UF/10V
C1408 1UF/6.3V
C1409 0.1UF/10V
C1410 10UF/10V
C1411 0.47UF/16V
VCC_AXG_1
VCC_AXG_2
VCC_AXG_3
VCC_AXG_4
VCC_AXG_5
VCC_AXG_6
VCC_AXG_7
VCC_AXG_8
VCC_AXG_9
VCC_AXG_10
VCC_AXG_11
VCC_AXG_12
VCC_AXG_13
VCC_AXG_14
VCC_AXG_15
VCC_AXG_16
VCC_AXG_17
VCC_AXG_18
VCC_AXG_19
VCC_AXG_20
VCC_AXG_21
VCC_AXG_22
VCC_AXG_23
VCC_AXG_24
VCC_AXG_25
VCC_AXG_26
VCC_AXG_27
VCC_AXG_28
VCC_AXG_29
VCC_AXG_30
VCC_AXG_31
VCC_AXG_32
VCC_AXG_33
VCC_AXG_34
VCC_AXG_35
VCC_AXG_36
VCC_AXG_37
VCC_AXG_38
VCC_AXG_39
VCC_AXG_40
VCC_AXG_41
VCC_AXG_42
VCC GFX
T1301
T1302
VCC_AXG_SENSE
VSS_AXG_SENSE
Route VCC_AXG_SENSE and VSS_AXG_SENSE differentially.
CANTIGA_CHIPSET
+VCCP
(Graph Core)
+VCCP_GFX
CE1403 100UF/2.5V
VCC_AXG_NCTF_1
VCC_AXG_NCTF_2
VCC_AXG_NCTF_3
VCC_AXG_NCTF_4
VCC_AXG_NCTF_5
VCC_AXG_NCTF_6
VCC_AXG_NCTF_7
VCC_AXG_NCTF_8
VCC_AXG_NCTF_9
VCC_AXG_NCTF_10
VCC_AXG_NCTF_11
VCC_AXG_NCTF_12
VCC_AXG_NCTF_13
VCC_AXG_NCTF_14
VCC_AXG_NCTF_15
VCC_AXG_NCTF_16
VCC_AXG_NCTF_17
VCC_AXG_NCTF_18
VCC_AXG_NCTF_19
VCC_AXG_NCTF_20
VCC_AXG_NCTF_21
VCC_AXG_NCTF_22
VCC_AXG_NCTF_23
VCC_AXG_NCTF_24
VCC_AXG_NCTF_25
VCC_AXG_NCTF_26
VCC_AXG_NCTF_27
VCC_AXG_NCTF_28
VCC_AXG_NCTF_29
VCC_AXG_NCTF_30
VCC_AXG_NCTF_31
VCC_AXG_NCTF_32
VCC_AXG_NCTF_33
VCC_AXG_NCTF_34
VCC_AXG_NCTF_35
VCC_AXG_NCTF_36
VCC_AXG_NCTF_37
VCC_AXG_NCTF_38
VCC_AXG_NCTF_39
VCC_AXG_NCTF_40
VCC_AXG_NCTF_41
VCC_AXG_NCTF_42
VCC_AXG_NCTF_43
VCC_AXG_NCTF_44
VCC_AXG_NCTF_45
VCC_AXG_NCTF_46
VCC_AXG_NCTF_47
VCC_AXG_NCTF_48
VCC_AXG_NCTF_49
VCC_AXG_NCTF_50
VCC_AXG_NCTF_51
VCC_AXG_NCTF_52
VCC_AXG_NCTF_53
VCC_AXG_NCTF_54
VCC_AXG_NCTF_55
VCC_AXG_NCTF_56
VCC_AXG_NCTF_57
VCC_AXG_NCTF_58
VCC_AXG_NCTF_59
VCC_AXG_NCTF_60
VCC GFX NCTF
VCC_SM_36
VCC_SM_37
VCC_SM_38
VCC_SM_39
VCC_SM_40
C1412 0.1UF/10V
C1413 0.1UF/10V
C1414 0.1UF/10V
C1415 0.1UF/10V
C1416 0.1UF/10V
VCC_SM_LF1
VCC_SM_LF2
VCC_SM_LF3
VCC_SM_LF4
VCC_SM_LF5
VCC_SM_LF6
VCC_SM_LF7
VCC SM LF
C1417 0.1UF/10V
C1418 0.1UF/10V
C1419 0.22UF/10V
C1420 0.22UF/10V
C1421 0.47UF/16V
C1422 1UF/6.3V
C1423 1UF/6.3V
+VCCP
Max : 2900mA(Core)
370 mils from the Edge
CE1404 100UF/2.5V
CE1405 100UF/2.5V
In Cavity
C1424 10UF/10V
C1425 10UF/10V N/A
At Edge Pin Location
C1426 0.1UF/10V
C1427 1UF/10V
At Package Edge
C1428 0.1UF/10V
C1429 0.1UF/10V
+VCCP_GMCH
U1001F
VCC_1
VCC_2
VCC_3
VCC_4
VCC_5
VCC_6
VCC_7
VCC_8
VCC_9
VCC_10
VCC_11
VCC_12
VCC_13
VCC_14
VCC_15
VCC_16
VCC_17
VCC_18
VCC_19
VCC_20
VCC_21
VCC_22
VCC_23
VCC_24
VCC_25
VCC_26
VCC_27
VCC_28
VCC_29
VCC_30
VCC_31
VCC_32
VCC_33
VCC_34
VCC_35
T32
VCC CORE
POWER
VCC_NCTF_1
VCC_NCTF_2
VCC_NCTF_3
VCC_NCTF_4
VCC_NCTF_5
VCC_NCTF_6
VCC_NCTF_7
VCC_NCTF_8
VCC_NCTF_9
VCC_NCTF_10
VCC_NCTF_11
VCC_NCTF_12
VCC_NCTF_13
VCC_NCTF_14
VCC_NCTF_15
VCC_NCTF_16
VCC_NCTF_17
VCC_NCTF_18
VCC_NCTF_19
VCC_NCTF_20
VCC_NCTF_21
VCC_NCTF_22
VCC_NCTF_23
VCC_NCTF_24
VCC_NCTF_25
VCC_NCTF_26
VCC_NCTF_27
VCC_NCTF_28
VCC_NCTF_29
VCC_NCTF_30
VCC_NCTF_31
VCC_NCTF_32
VCC_NCTF_33
VCC_NCTF_34
VCC_NCTF_35
VCC_NCTF_36
VCC_NCTF_37
VCC_NCTF_38
VCC_NCTF_39
VCC_NCTF_40
VCC_NCTF_41
VCC_NCTF_42
VCC_NCTF_43
VCC_NCTF_44
VCC NCTF
+VCCP_GMCH
CANTIGA_CHIPSET
ASUSTeK COMPUTER INC. NB1
Title : Cantiga--POWER (4)
Engineer: <OrgAddr1>
Size Custom
Project Name N50A/N51A
Rev 1.0
Date: Thursday, July 24, 2008
Sheet 14 of 79
WWW.AliSaler.Com



ASUSTeK COMPUTER INC. NB1	Title : Cantiga-POWER(5)		
	Engineer: <OrgAddr1>		
Size: Custom	Project Name: N50A/N51A		Rev: 1.0
Date: Tuesday, July 29, 2008	Sheet 15 of 79		



R1.1_(4)



ASUSTeK COMPUTER INC. NB1

Title : Cantiga-GND

Engineer: <OrgAddr1>

Size	Project Name	Rev
C	N50A/N51A	1.0

Date: Friday, August 01, 2008 Sheet 16 of 79

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ASUSTeK COMPUTER INC. NB1	Title : Engineer: <OrgAddr1>	
Size: A	Project Name: N50A/N51A	Rev: 1.0
Date: Thursday, July 24, 2008	Sheet 17 of 79	

Title :		
ASUSTeK COMPUTER INC. NB1	Engineer: <OrgAddr1>	
Size: B	Project Name: N50A/N51A	Rev: 1.0
Date: Thursday, July 24, 2008	Sheet 18 of 79	

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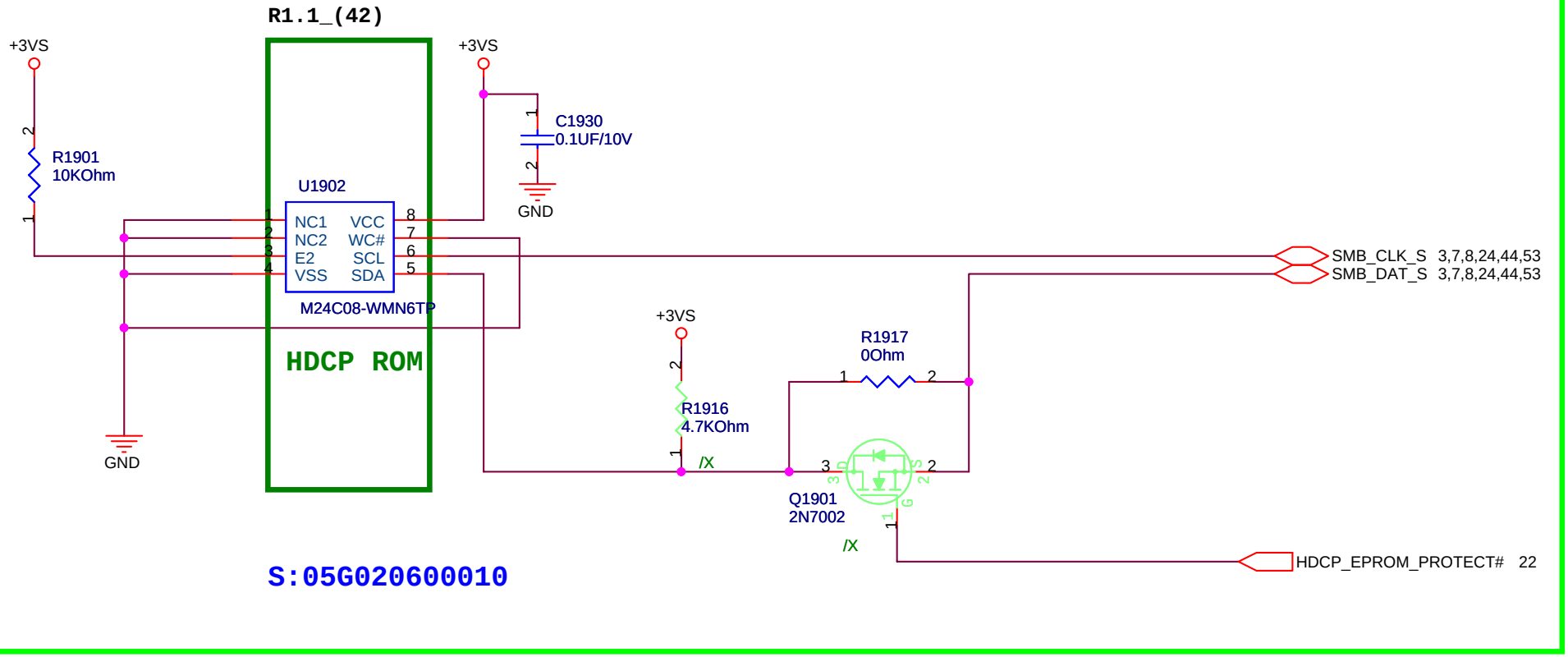
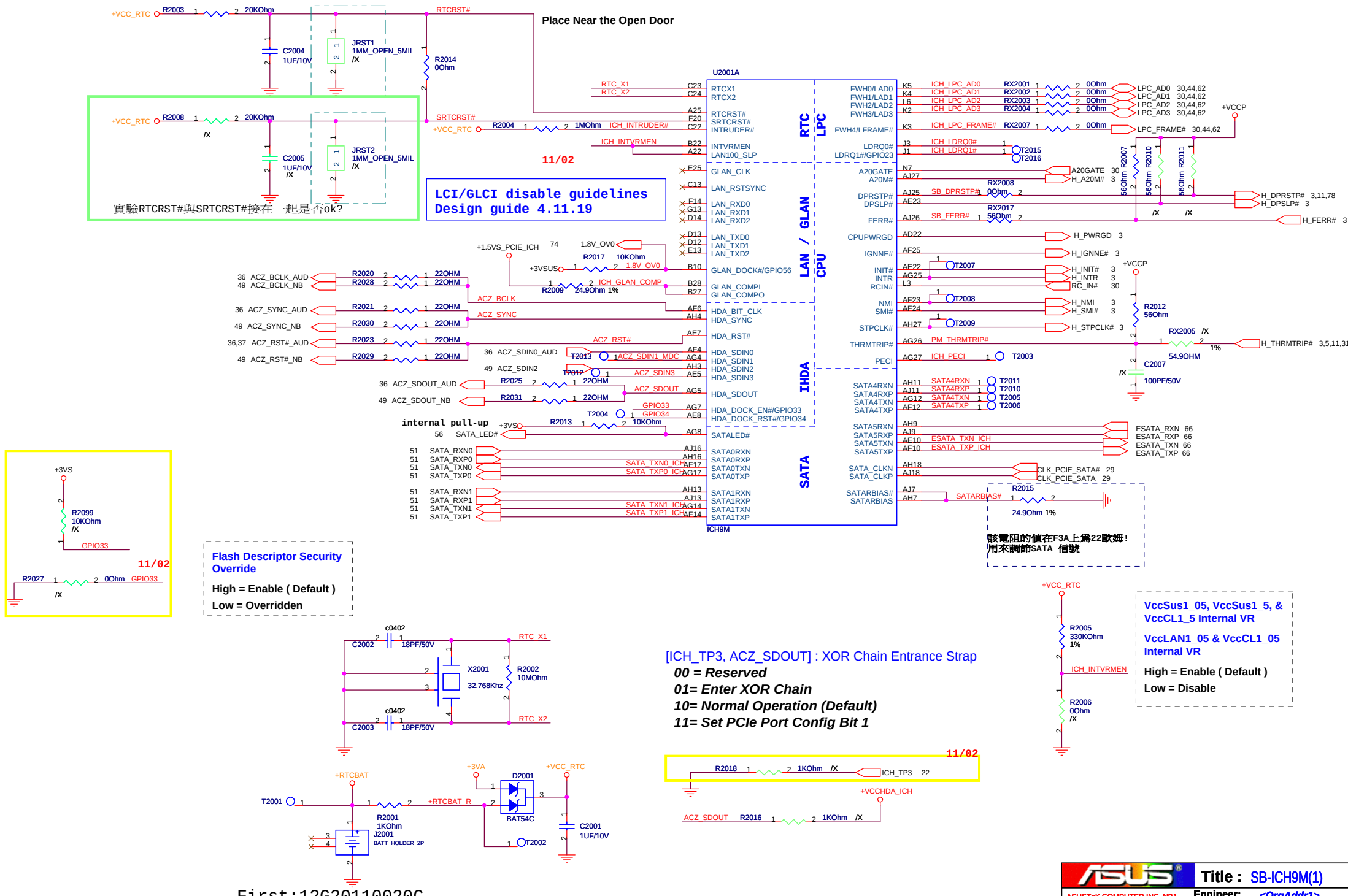
R1.1_(11)

R1.1_(42)



S:05G020600010

ASUSTeK COMPUTER INC. NB1	Title :	
	Engineer: <OrgAddr1>	
Size: A	Project Name: N50A/N51A	Rev: 1.0
Date: Friday, August 01, 2008	Sheet 19 of 79	


Place Near the Open Door
11/02
實驗RTCRST#與SRTCRST#接在一起是否ok?
LCI/GLCI disable guidelines
Design guide 4.11.19
U2001A
ICH9M
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
internal pull-up
Flash Descriptor Security Override
High = Enable (Default)
Low = Overridden
[ICH_TP3, ACZ_SDOUT] : XOR Chain Entrance Strap
00 = Reserved
01= Enter XOR Chain
10= Normal Operation (Default)
11= Set PCIe Port Config Bit 1
VccSus1_05, VccSus1_5, & VccCL1_5 Internal VR
VccLAN1_05 & VccCL1_05 Internal VR
High = Enable (Default)
Low = Disable
R2027 0Ohm GPIO33
/X
R2018 1KOhm /X ICH_TP3
ACZ_SDOUT R2016 1KOhm /X
R2005 330KOhm 1%
R2006 0Ohm /X
ICH_INTVRMEN
+VCC_RTC
+VCCHDA_ICH
+RTCBAT
+3VA
+3VS
+VCCP
+1.5VS_PCIE_ICH
+3VSUS
1.8V_OV0
ICH_GLAN_COMP
ACZ_BCLK
ACZ_SYNC
ACZ_RST#
ACZ_SDOUT
ACZ_SDIN1_MDC
ACZ_SDIN3
GPIO33
GPIO34
SATA_LED#
SATA_TXN0_ICH
SATA_TXP0_ICH
SATA_TXN1_ICH
SATA_TXP1_ICH
ESATA_RXN
ESATA_RXP
ESATA_TXN
ESATA_TXP
ESATA_TXN_ICH
ESATA_TXP_ICH
CLK_PCIE_SATA#
CLK_PCIE_SATA
SATARBIAS#
RTC_X1
RTC_X2
RTCRST#
SRTCRST#
ICH_INTRUDER#
ICH_INTVRMEN
H_PWRGD
H_IGNNE#
H_INIT#
H_INTR
RC_IN#
H_NMI
H_SMI#
H_STPCLK#
H_THRMTRIP#
H_DPRSTP#
H_DPSLP#
H_FERR#
PM_THRMTRIP#
ICH_PECI
SB_DPRSTP#
SB_FERR#
A20GATE
H_A20M#
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LPC_FRAME#
ICH_LPC_AD0
ICH_LPC_AD1
ICH_LPC_AD2
ICH_LPC_AD3
ICH_LPC_FRAME#
ICH_LDRQ0#
ICH_LDRQ1#
R2001 R2002 R2003 R2004 R2007
R2008 R2009 R2010 R2011 R2012 R2013 R2014 R2015 R2017
RX2001 RX2002 RX2003 RX2004 RX2005 RX2007 RX2008 RX2017
C2001 C2002 C2003 C2004 C2005 C2007
JRST1 JRST2
X2001 32.768Khz
D2001 BAT54C
J2001 BATT_HOLDER_2P
T2001 T2002 T2003 T2004 T2005 T2006 T2007 T2008 T2009 T2010 T2011 T2012 T2013 T2015 T2016
54.9OHM
100PF/50V
First:12G20110020C
second:12G201100208
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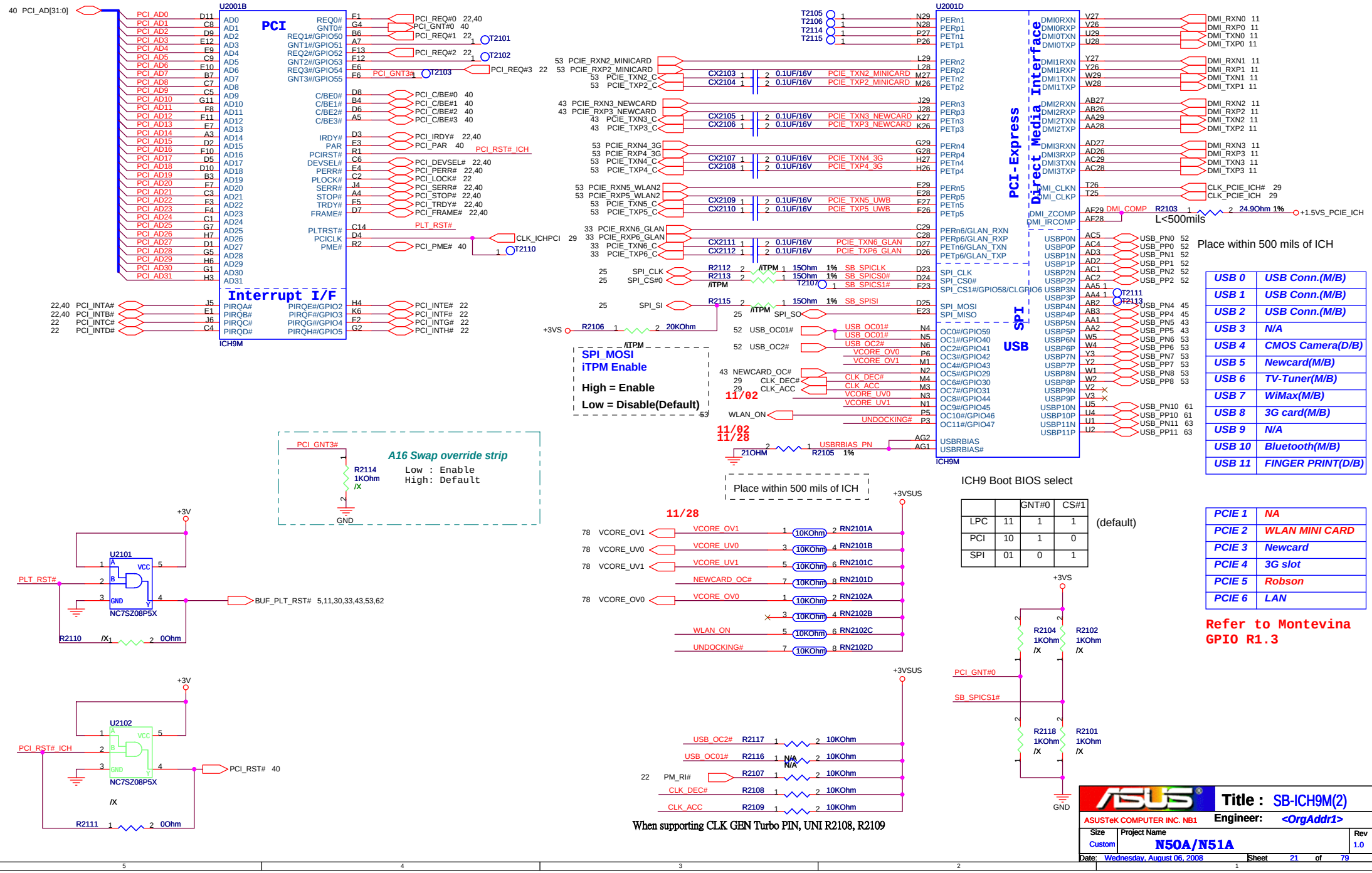
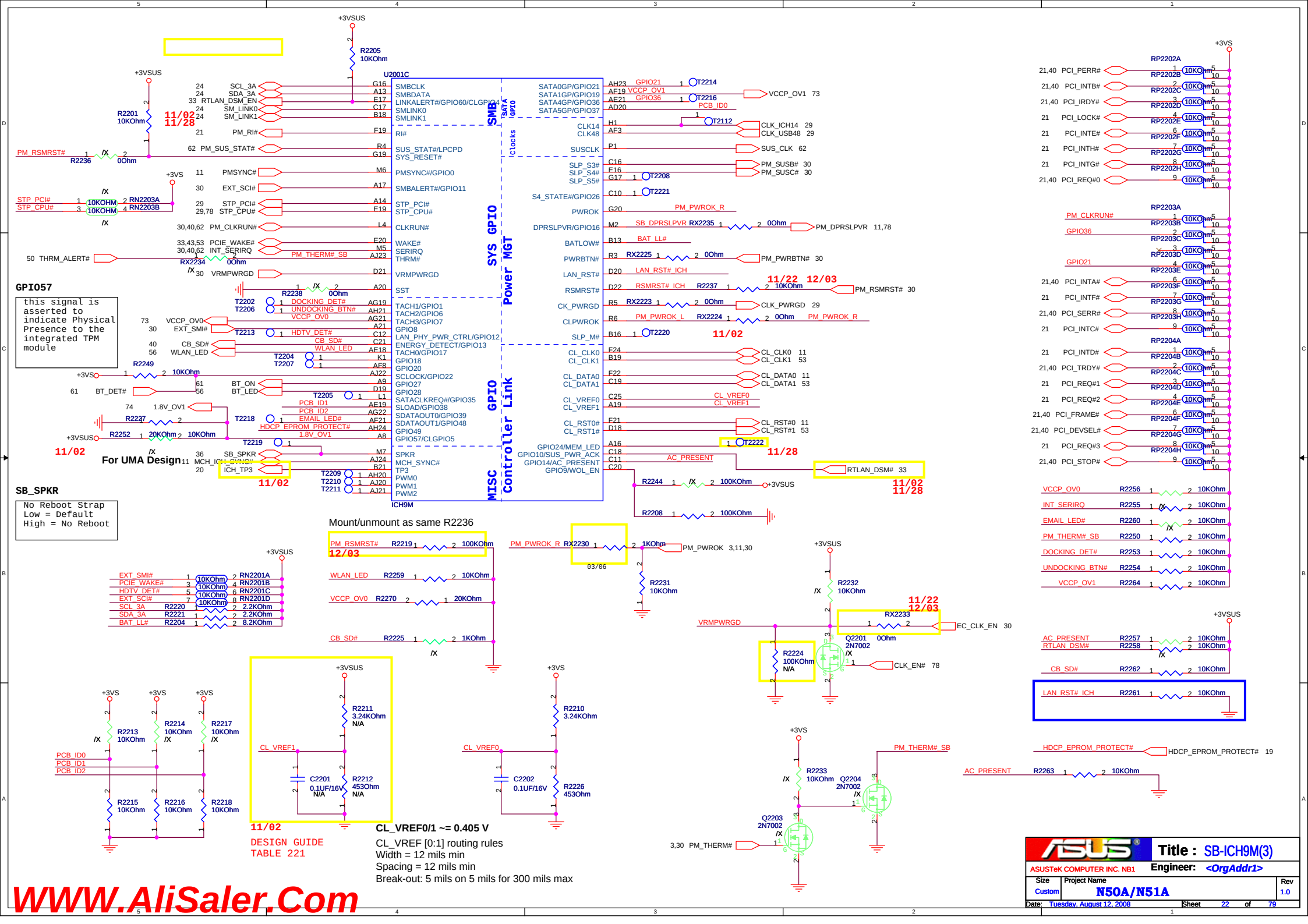
ASUSTeK COMPUTER INC. NB1
Title : SB-ICH9M(1)
Engineer: <OrgAddr1>
Size Custom
Project Name N50A/N51A
Rev 1.0
Date: Friday, August 01, 2008
Sheet 20 of 79



		GNT#0	CS#1
LPC	11	1	1
PCI	10	1	0
SPI	01	0	1

USB 0	USB Conn.(M/B)
USB 1	USB Conn.(M/B)
USB 2	USB Conn.(M/B)
USB 3	N/A
USB 4	CMOS Camera(D/B)
USB 5	Newcard(M/B)
USB 6	TV-Tuner(M/B)
USB 7	WiMax(M/B)
USB 8	3G card(M/B)
USB 9	N/A
USB 10	Bluetooth(M/B)
USB 11	FINGER PRINT(D/B)

PCIE 1	NA
PCIE 2	WLAN MINI CARD
PCIE 3	Newcard
PCIE 4	3G slot
PCIE 5	Robson
PCIE 6	LAN


U2001C
ICH9M
SMB
SATA GPIO
Clocks
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
SMBCLK
SMBDATA
LINKALERT#/GPIO60/CLGPIO4
SMLINK0
SMLINK1
RI#
SUS_STAT#/LPCPD
SYS_RESET#
CLKRUN#
WAKE#
SERIRQ
THRM#
VRMPWRGD
SST
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
LAN_PHY_PWR_CTRL/GPIO12
ENERGY_DETECT/GPIO13
TACH0/GPIO17
GPIO18
GPIO20
SCLOCK/GPIO22
GPIO27
GPIO28
SATACLKREQ#/GPIO35
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
GPIO49
GPIO57/CLGPIO5
SPKR
MCH_SYNC#
TP3
PWM0
PWM1
PWM2
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA4GP/GPIO36
SATA5GP/GPIO37
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
S4_STATE#/GPIO26
PWROK
DPRSLPVR/GPIO16
BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
CK_PWRGD
CLPWROK
SLP_M#
CL_CLK0
CL_CLK1
CL_DATA0
CL_DATA1
CL_VREF0
CL_VREF1
CL_RST0#
CL_RST1#
GPIO24/MEM_LED
GPIO10/SUS_PWR_ACK
GPIO14/AC_PRESENT
GPIO9/WOL_EN
GPIO057
this signal is asserted to indicate Physical Presence to the integrated TPM module
SB_SPKR
No Reboot Strap
Low = Default
High = No Reboot
For UMA Design
Mount/unmount as same R2236
DESIGN GUIDE TABLE 221
CL_VREF0/1 ~= 0.405 V
CL_VREF [0:1] routing rules
Width = 12 mils min
Spacing = 12 mils min
Break-out: 5 mils on 5 mils for 300 mils max
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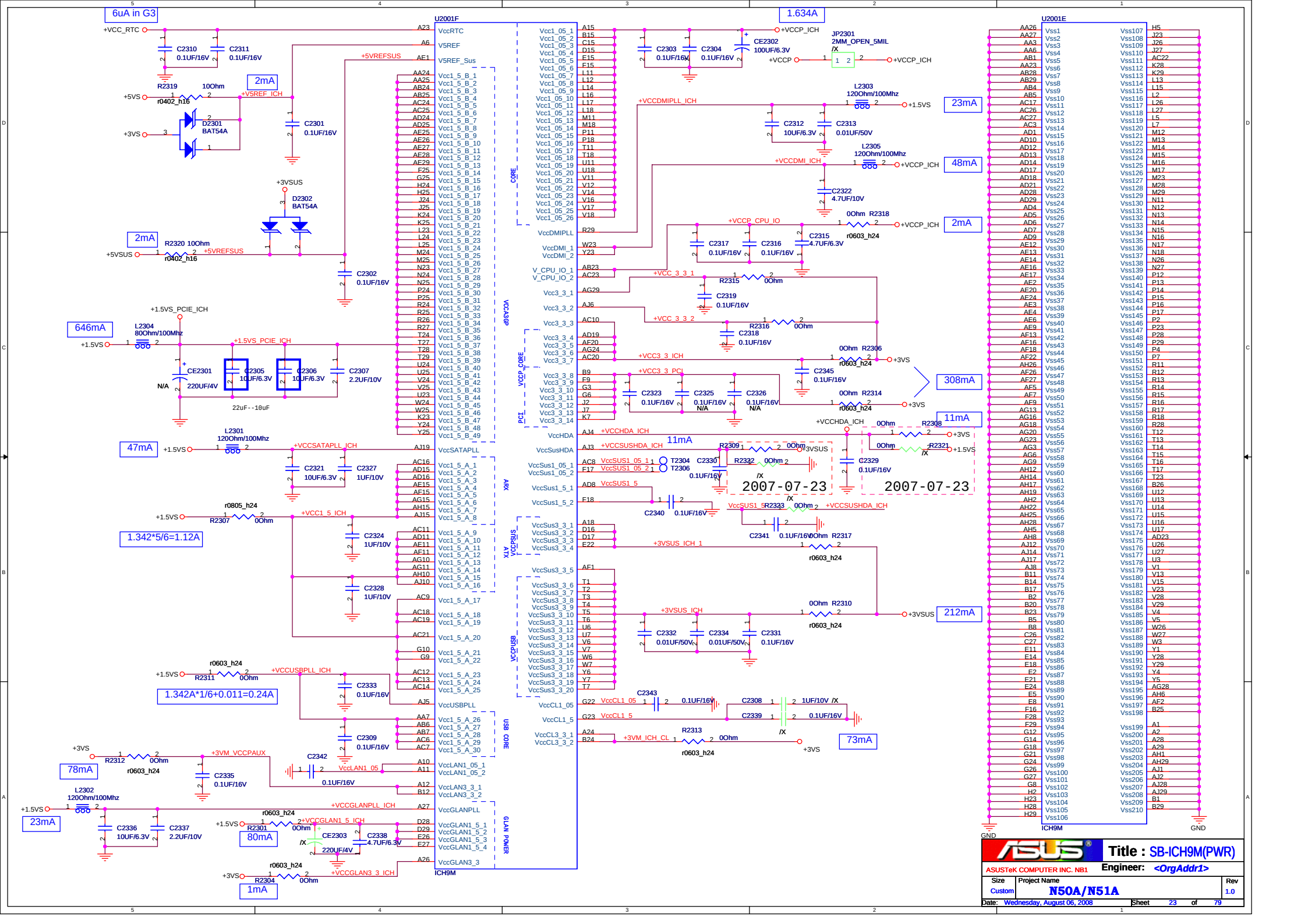
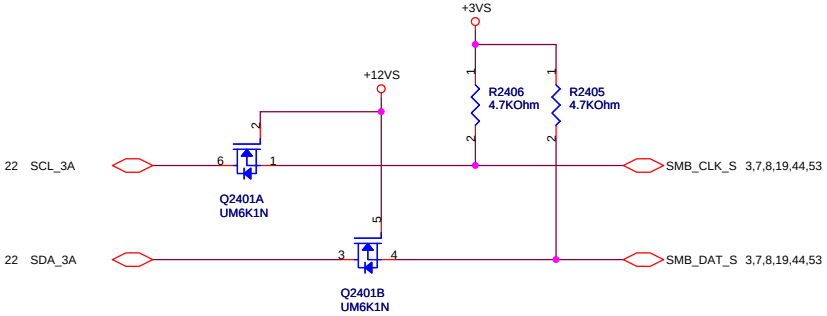
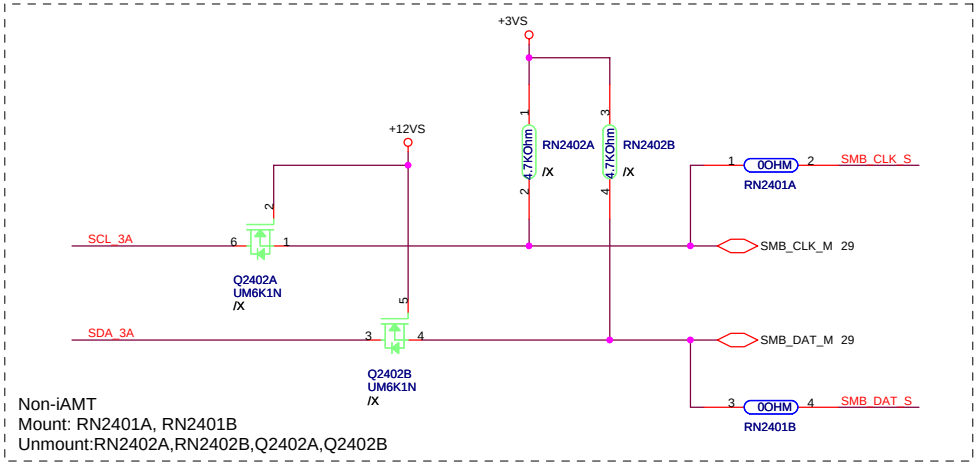
ASUSTeK COMPUTER INC. NB1
Title : SB-ICH9M(3)
Engineer: <OrgAddr1>
Size Custom
Project Name N50A/N51A
Rev 1.0
Date: Tuesday, August 12, 2008
Sheet 22 of 79


6uA in G3
1.634A
U2001F
U2001E
ICH9M
+VCC_RTC
C2310 0.1UF/16V
C2311 0.1UF/16V
2mA
R2319 10Ohm
r0402_h16
+5VS
+3VS
D2301 BAT54A
C2301 0.1UF/16V
+5VREFSUS
+5VREF_ICH
+3VSUS
D2302 BAT54A
R2320 10Ohm
+5VSUS
C2302 0.1UF/16V
+1.5VS_PCIE_ICH
646mA
L2304 80Ohm/100Mhz
+1.5VS
CE2301 220UF/4V
C2305 10UF/6.3V
C2306 10UF/6.3V
C2307 2.2UF/10V
22uF--10uF
47mA
L2301 120Ohm/100Mhz
+VCCSATAPLL_ICH
C2321 10UF/6.3V
C2327 1UF/10V
r0805_h24
R2307 0Ohm
+VCC1_5_ICH
1.342*5/6=1.12A
C2324 1UF/10V
C2328 1UF/10V
r0603_h24
R2311 0Ohm
+VCCUSBPLL_ICH
1.342A*1/6+0.011=0.24A
C2333 0.1UF/16V
C2309 0.1UF/16V
+3VS
R2312 0Ohm
r0603_h24
78mA
+3VM_VCCPAUX
C2335 0.1UF/16V
C2342 0.1UF/16V
VccLAN1_05
L2302 120Ohm/100Mhz
+1.5VS
23mA
C2336 10UF/6.3V
C2337 2.2UF/10V
+VCCGLANPLL_ICH
R2301 0Ohm
80mA
+VCCGLAN1_5_ICH
CE2303 220UF/4V
C2338 4.7UF/6.3V
+3VS
R2304 0Ohm
+VCCGLAN3_3_ICH
1mA
CORE
VCC3GP
VCCP_CORE
PCI
ARX
VCCPSUS
AUX
VCCPUSB
USB CORE
GLAN POWER
C2303 0.1UF/16V
C2304 0.1UF/16V
CE2302 100UF/6.3V
+VCCP_ICH
JP2301 2MM_OPEN_5MIL
+VCCP
+VCCDMIPLL_ICH
L2303 120Ohm/100Mhz
+1.5VS
23mA
C2312 10UF/6.3V
C2313 0.01UF/50V
+VCCDMI_ICH
L2305 120Ohm/100Mhz
48mA
C2322 4.7UF/10V
+VCCP_CPU_IO
0Ohm R2318
2mA
C2317 0.1UF/16V
C2316 0.1UF/16V
C2315 4.7UF/6.3V
+VCC_3_3_1
R2315 0Ohm
C2319 0.1UF/16V
+VCC_3_3_2
R2316 0Ohm
C2318 0.1UF/16V
+VCC3_3_ICH
0Ohm R2306
308mA
C2345 0.1UF/16V
+VCC3_3_PCI
C2323 0.1UF/16V
C2325 0.1UF/16V
C2326 0.1UF/16V
N/A
0Ohm R2314
+VCCHDA_ICH
0Ohm R2308
11mA
+VCCSUSHDA_ICH
R2309 0Ohm
R2321 /X
C2329 0.1UF/16V
2007-07-23
T2304
T2306
C2330 0.1UF/16V
R2332 0Ohm
VccSUS1_05_1
VccSUS1_05_2
VccSUS1_5
C2340 0.1UF/16V
R2333 0Ohm
C2341 0.1UF/16V
R2317 0Ohm
+3VSUS_ICH_1
+3VSUS_ICH
0Ohm R2310
212mA
C2332 0.01UF/50V
C2334 0.01UF/50V
C2331 0.1UF/16V
C2343 0.1UF/16V
VccCL1_05
C2308 1UF/10V /X
C2339 0.1UF/16V
VccCL1_5
R2313 0Ohm
+3VM_ICH_CL
73mA
GND
ASUSTeK COMPUTER INC. NB1
Title : SB-ICH9M(PWR)
Engineer: <OrgAddr1>
Size Custom
Project Name N50A/N51A
Rev 1.0
Date: Wednesday, August 06, 2008
Sheet 23 of 79

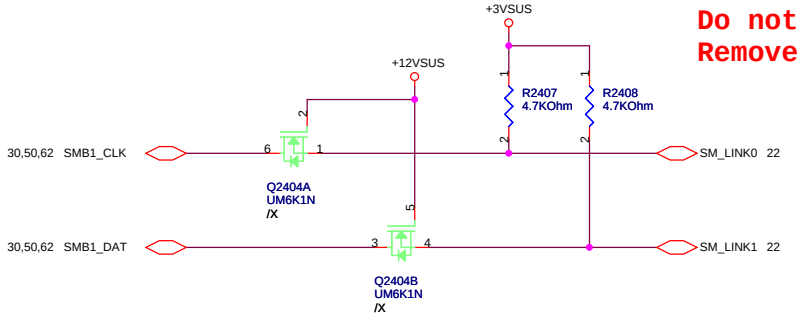
ICH9-M





Non-iAMT
Mount: RN2401A, RN2401B
Unmount:RN2402A,RN2402B,Q2402A,Q2402B

EC-IT8752



Do not support iAMT
Remove ME-EC smbus

Master	Slave
SCL_3A SDA_3A (ICH9M)	A. SMB_CLK_S SMB_DAT_S → SO-DIMM0; SO-DIMM1; Debug; WLAN Card B. SMB_CLK_M SMB_DAT_M → CLK Generator
SMB0_CLK SMB0_DAT (EC)	BATTERY
SMB1_CLK SMB1_DAT (EC)	Thermal Sensor

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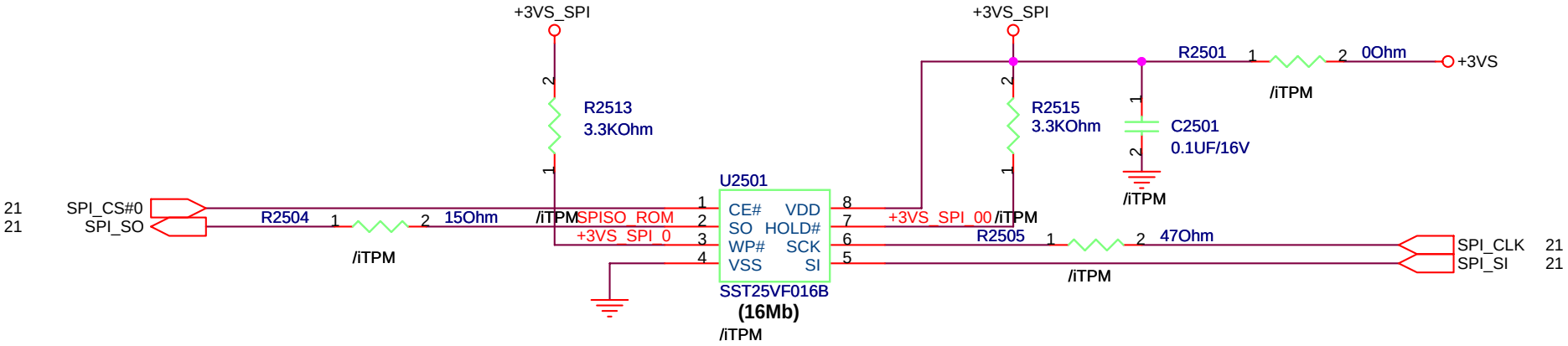
ASUSTeK COMPUTER INC. NB1	Title : ICH9M-Other	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50A/N51A	Rev: 1.0
Date: Friday, August 01, 2008	Sheet 24 of 79	



FOR iTPM
8Mb 05G00120A010

ASUSTeK COMPUTER INC. NB1	Title : SPI ROM	
	Engineer: <OrgAddr1>	
Size: A	Project Name: N50A/N51A	Rev: 1.0
Date: Wednesday, August 06, 2008	Sheet 25 of 79	

ASUSTeK COMPUTER INC. NB1	Title :		
	Engineer: <OrgAddr1>		
Size: A	Project Name: N50A/N51A		Rev: 1.0
Date: Thursday, July 24, 2008	Sheet 26 of 79		

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ASUSTeK COMPUTER INC. NB1	Title : Engineer: <OrgAddr1>	
Size: A	Project Name: N50A/N51A	Rev: 1.0
Date: Thursday, July 24, 2008	Sheet 27 of 79	

ASUSTeK COMPUTER INC. NB1	Title : Engineer: <OrgAddr1>	
Size: A	Project Name: N50A/N51A	Rev: 1.0
Date: Thursday, July 24, 2008	Sheet 28 of 79	

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2 source:RTM875T-363 06G011501020

U2901

ICS9LPR363EGLF-T

PEREQ#1
0: Enable control SATACLK & PCIEX0 / 6 through I2C
1: Disable SATACLK & PCIEX0 / 6 Controlled

PEREQ#2
0: Enable control PCIEX 1 / 8 through I2C
1: Disable PCIEX1/8 Controlled

PEREQ#3
0: Enable control PCIEX 4 / 2 through I2C
1: Disable PCIEX 4 / 2 Controlled

PEREQ#4
0: Enable control PCIEX 7 / 5 / 3 through I2C
1: Disable PCIEX 7 / 5 / 3 Controlled

Latched Input Select

Decide pin 43/44
0 = SRC CLK
1 = CPU_ITP CLK
(Pin8)
ITP_EN

Decide pin 17/18
0 = LCDCLK
1 = PCIEX
(Pin5)
SELPCIE0_LCD#

Decide pin 40/41
0 = PCIECLK
1 = PEREQ#
(Pin64)
REQ_SEL#

Decide pin 17/18
SELLCD_27# = 0:
pin14/15=PCIEX_9L
pin17/18=27FIX/27SS
SELLCD_27# = 1:
pin14/15=DOT_96MHzL
pin17/18=LCD_SSCG/PCIe_L0
(Pin9)

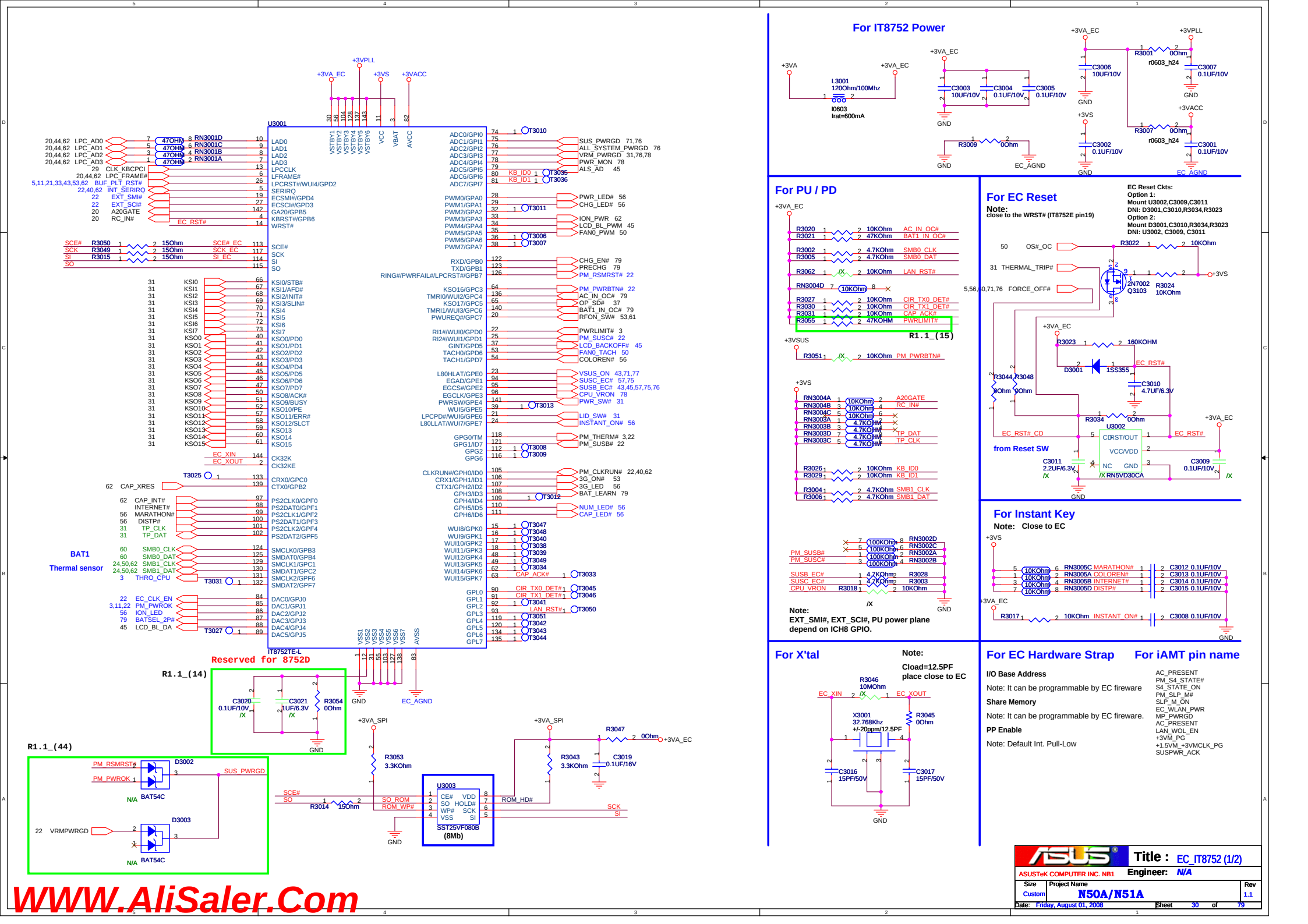
Pin5	Pin9	Pin14/15	Pin17/18
SELPCIEX0_LCD#/ PCI3 = 0 (low)	SELLCD_27#=0	PCIEX9 DOT96	27FIXSS LCD
	SELLCD_27#=1		
SELPCIEX0_LCD#/ PCI3 = 1 (high)	SELLCD_27#=0	PCIEX9	PCIEX0
	SELLCD_27#=1	DOT96	PCIEX0

	R2902	R2903	R2920
363: VREF	1K	330	UNI
364: TURBO	UNI	10K	0
364:NO TBO	UNI	UNI	UNI

BCLK	FSB	FSLC BSEL2	FSLB BSEL1	FSLA BSEL0
166	667	0	1	1
200	800	0	1	0
266	1066	0	0	0

Int PU/PD R=120K ohm.
Int PU: pin 5,9,32,33,34
Ext PD: pin 64

ASUSTeK COMPUTER INC. NB1
Title : CLOCK GEN
Engineer: <OrgAddr1>
Size: Custom
Project Name: N50A/N51A
Rev: 1.0
Date: Tuesday, August 05, 2008
Sheet 29 of 79



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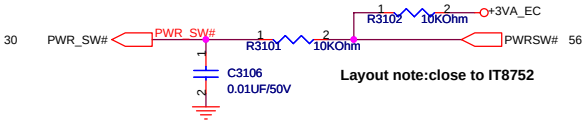
For Battery

Note: When plug in or out the battery, it may cause a spike to damage EC and gas gauge. It needs to add varistors to protect those pins.

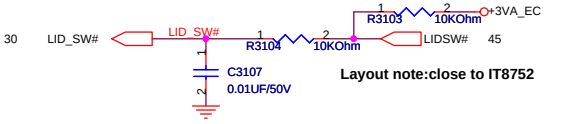
In Page 60

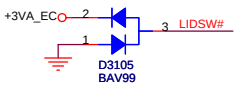
For Switch

PWR SWITCH



LID SWITCH



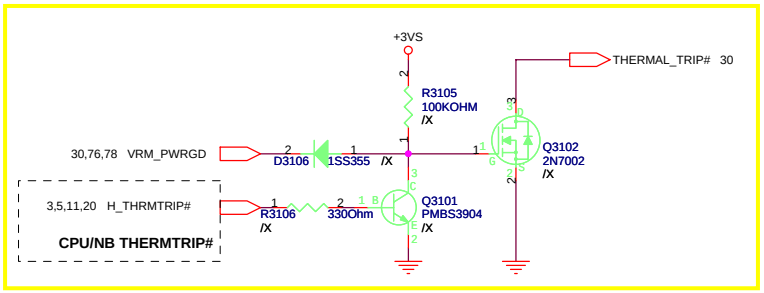


close to connector

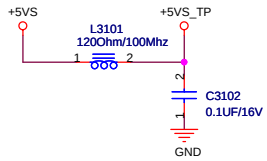
Note:
LID_SW# is easy to cause high voltage damage when plugging inverter board connector to M/B with AC present. Need to add bidirectional diode to protect this pin.

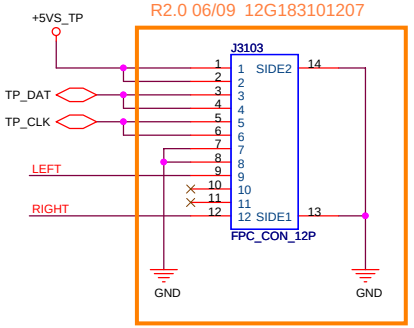
For Thermal Control Method

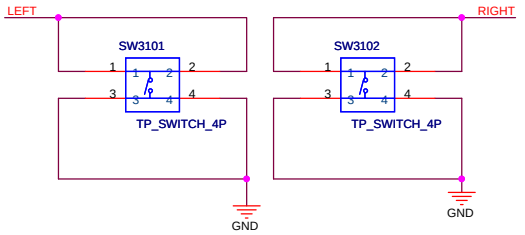
11/20 Remove redundant components

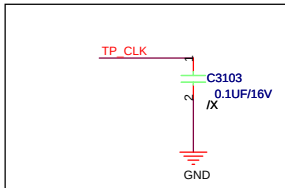


Touchpad Connector

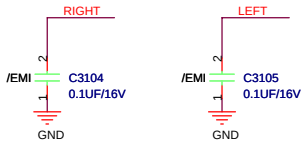




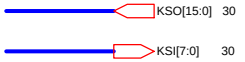




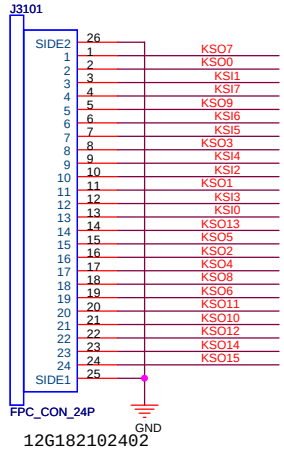
EMI 01/17 close to J3102



Keyboard Connector

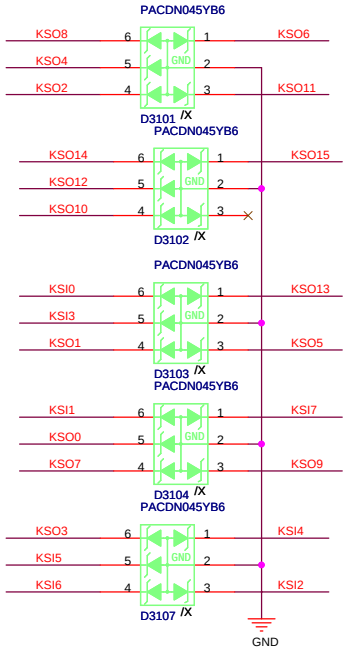


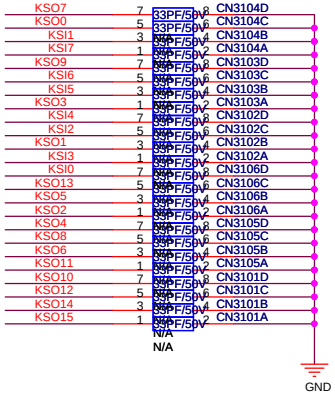
F7/N1 Keyboard



12G182102402

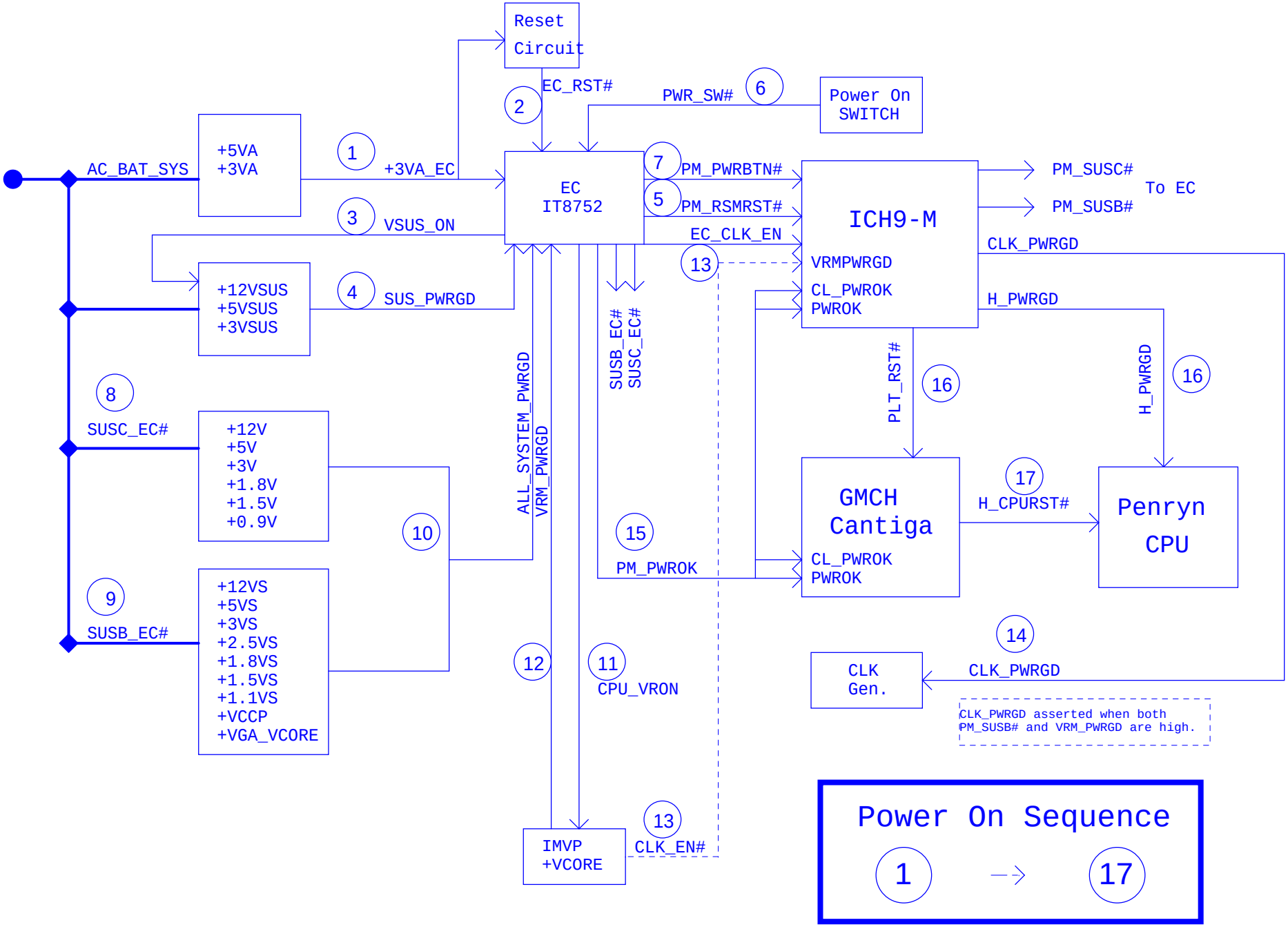
11/02





12G09103004P

ASUSTeK COMPUTER INC. NB1	Title : EC_IT8511 (2/2)		
	Engineer: <OrgAddr1>		
Size: Custom	Project Name: N50A/N51A		Rev: 1.0
Date: Wednesday, August 06, 2008	Sheet 31 of 79		



ASUSTeK COMPUTER INC. NB1	Title : POWER-ON SEQUENCE	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50A/N51A	Rev: 1.0
Date: Thursday, July 24, 2008	Sheet 32 of 79	

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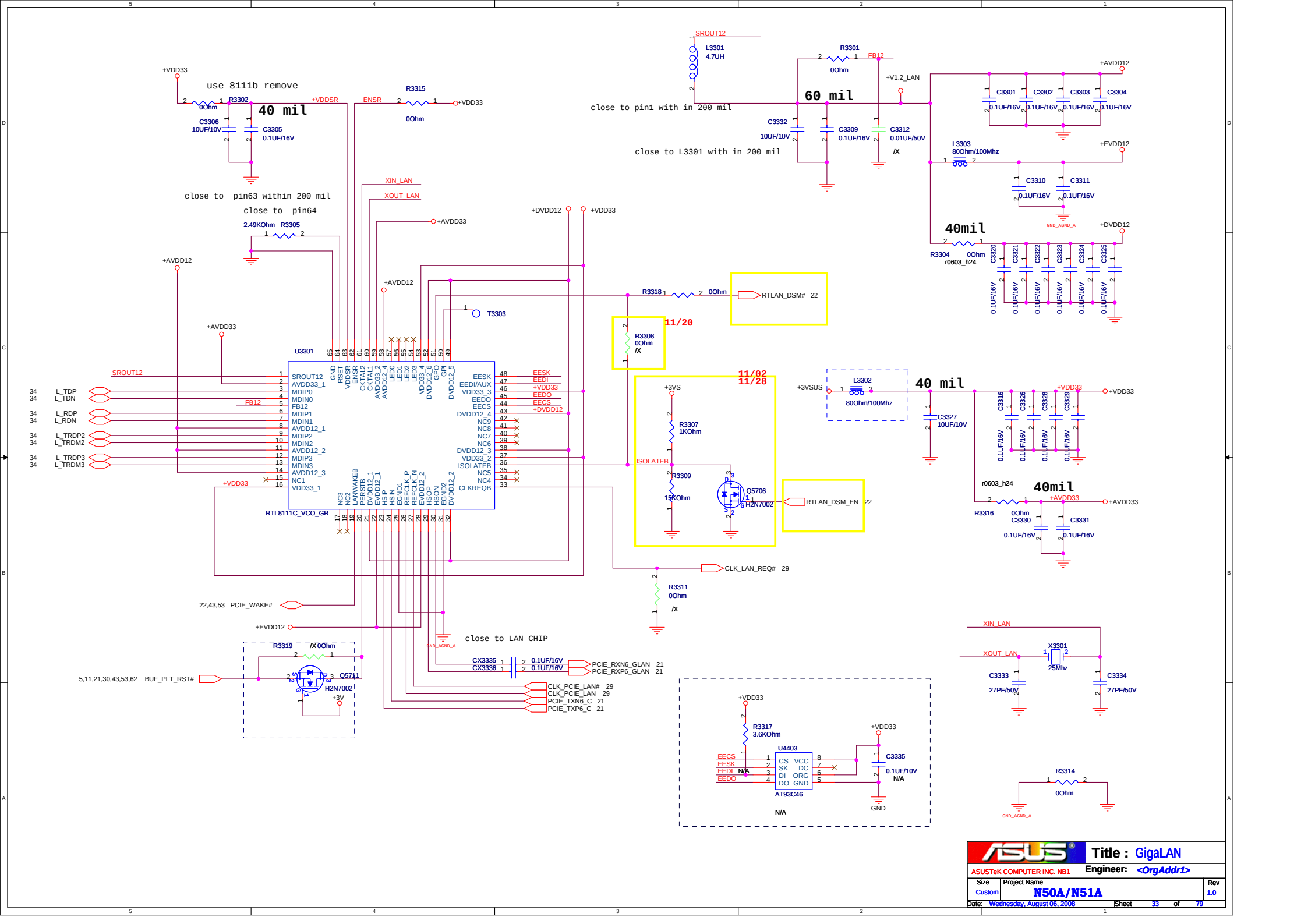
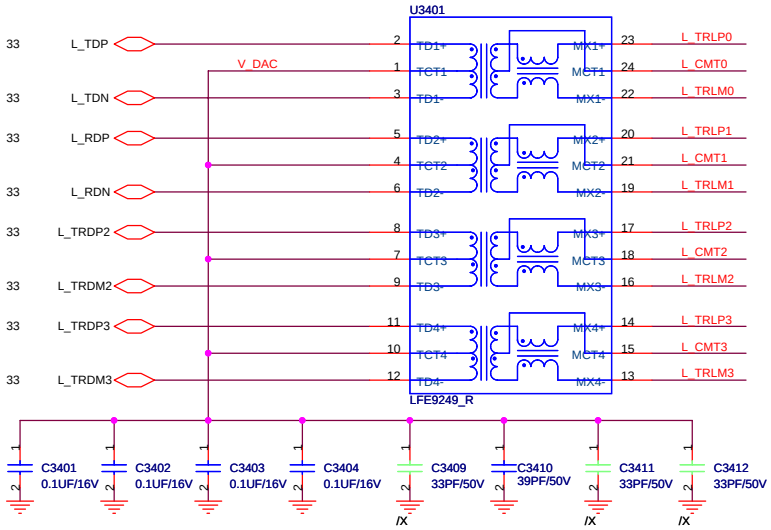
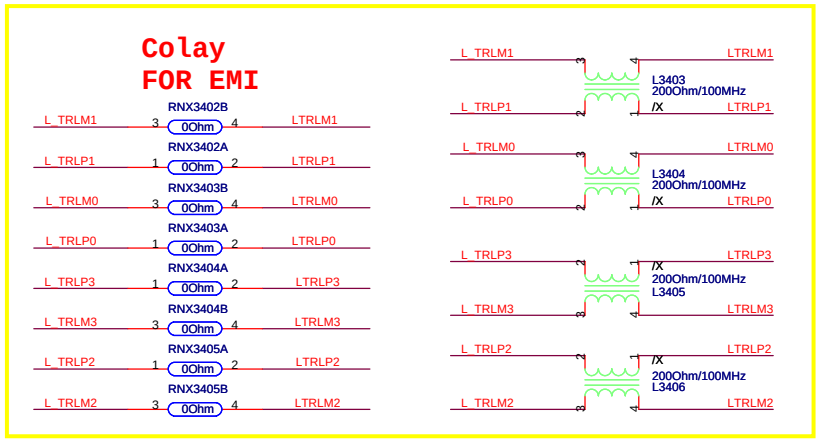
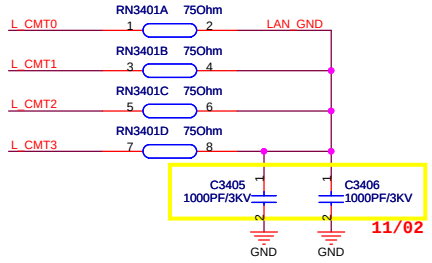
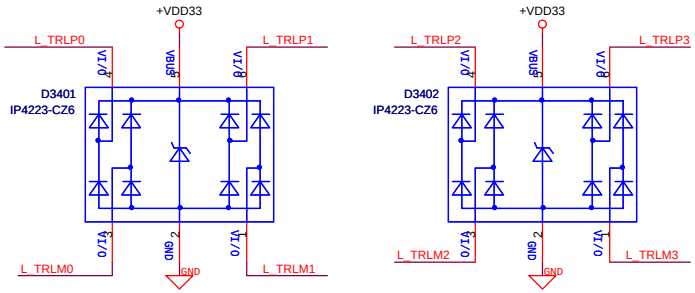
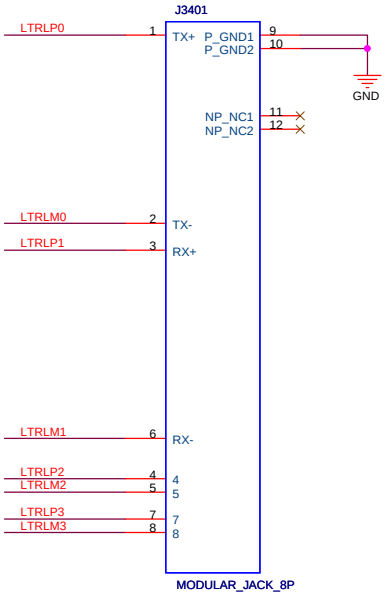

use 8111b remove
40 mil
close to pin63 within 200 mil
close to pin64
close to pin1 with in 200 mil
60 mil
close to L3301 with in 200 mil
40mil
11/20
11/02
11/28
close to LAN CHIP
RTL8111C_VCO_GR
U3301
T3303
U4403
AT93C46
Q5706
Q5711
H2N7002
RTLAN_DSM# 22
RTLAN_DSM_EN 22
CLK_LAN_REQ# 29
22,43,53 PCIE_WAKE#
5,11,21,30,43,53,62 BUF_PLT_RST#
PCIE_RXN6_GLAN 21
PCIE_RXP6_GLAN 21
CLK_PCIE_LAN# 29
CLK_PCIE_LAN 29
PCIE_TXN6_C 21
PCIE_TXP6_C 21
Title : GigaLAN
ASUSTeK COMPUTER INC. NB1
Engineer: <OrgAddr1>
Project Name N50A/N51A
Rev 1.0
Date: Wednesday, August 06, 2008
Sheet 33 of 79











12G142111083

ASUSTeK COMPUTER INC. NB1		Title : RJ45	
		Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50A/N51A		Rev: 1.0
Date: Friday, August 01, 2008		Sheet 34 of 79	

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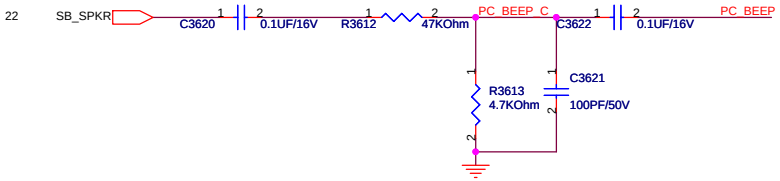
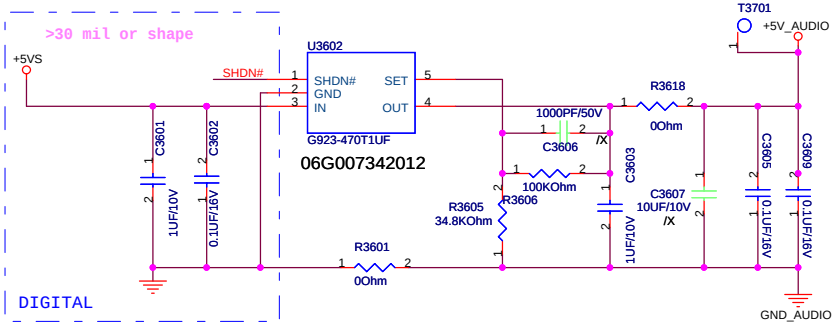
Title :	MDC
ASUSTeK COMPUTER INC. NB1	Engineer: <OrgAddr1>
Size: Custom	Project Name: N50A/N51A
Rev: 1.0	
Date: Thursday, July 24, 2008	Sheet 35 of 79

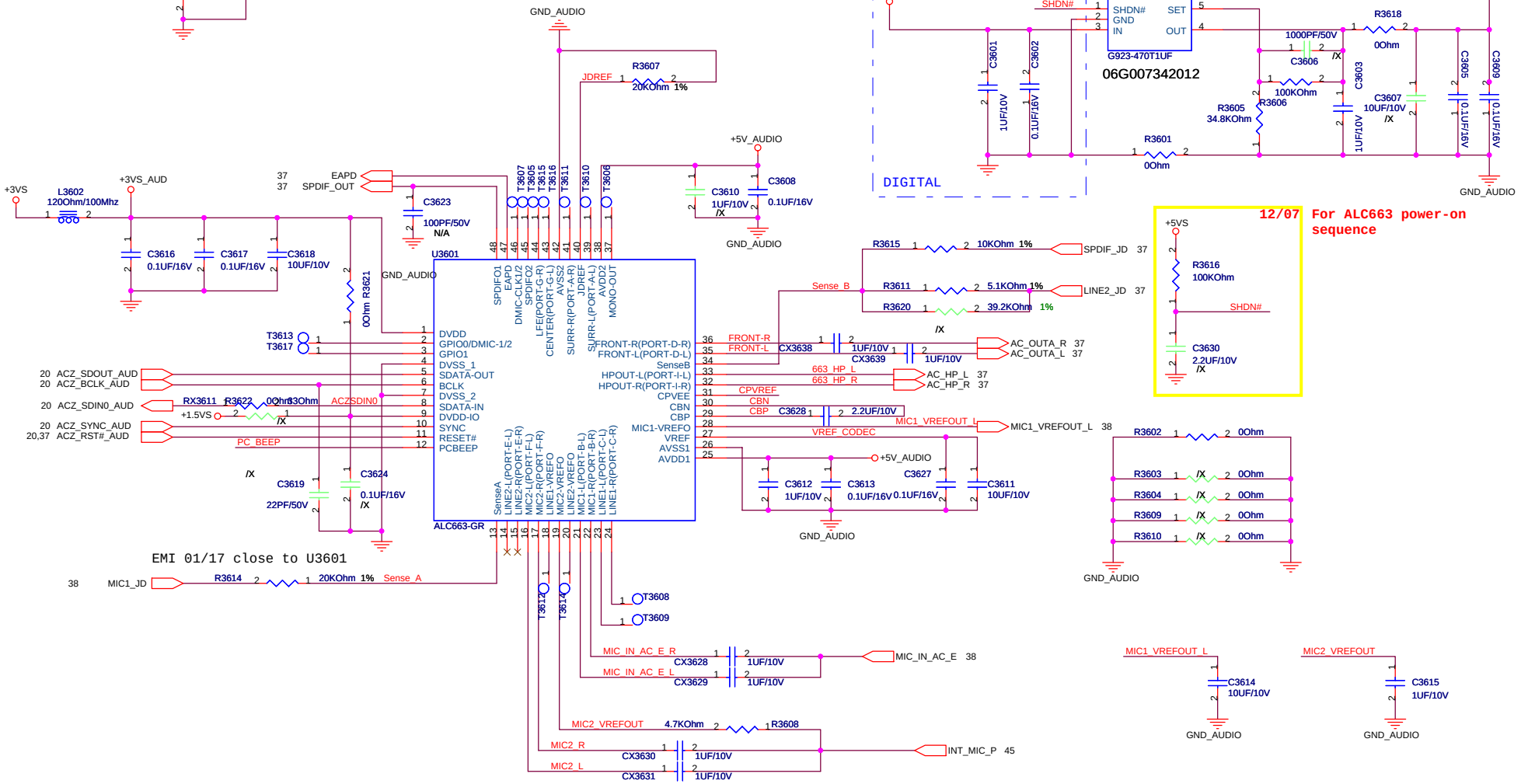
PC BEEP



Audio Power

FOR ADJUST MODE:
Vo=1.25*(1+R3706/R3705)
= 1.25*(1+ 100K/34.8K) = 4.84





Input impedence:64K ohm(Typical)

12/07 ALC663 CHARGE PUMP

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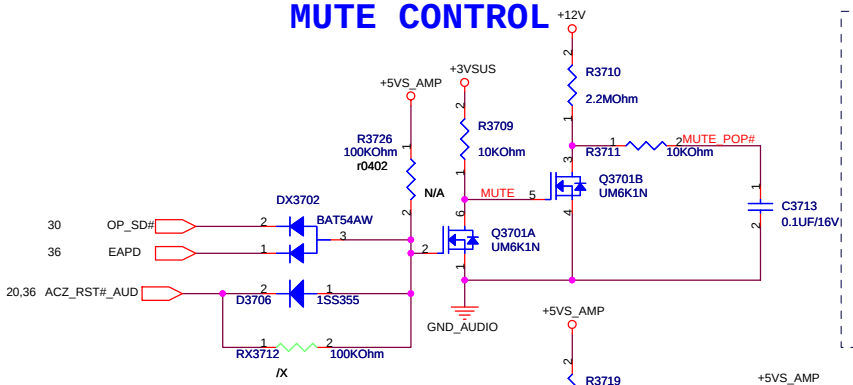
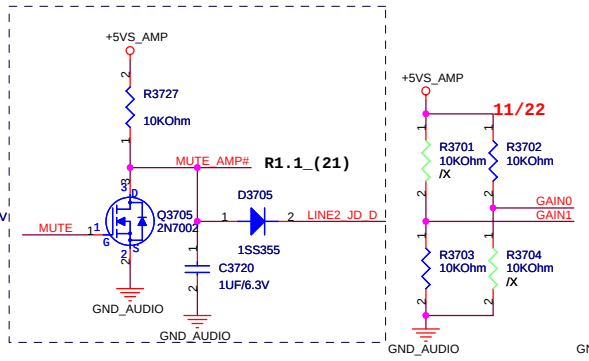
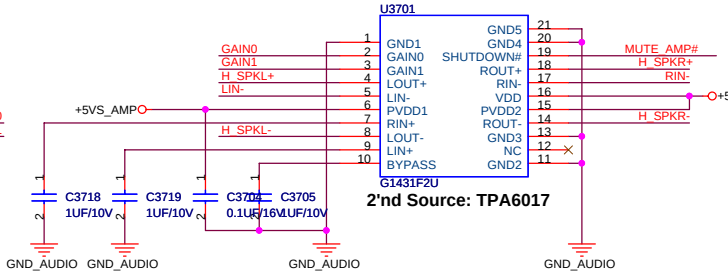
ASUSTeK COMPUTER INC. NB1	Title : CODEC ALC663	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50A/N51A	Rev: 1.0
Date: Wednesday, August 06, 2008	Sheet 36 of 79	

MUTE CONTROL

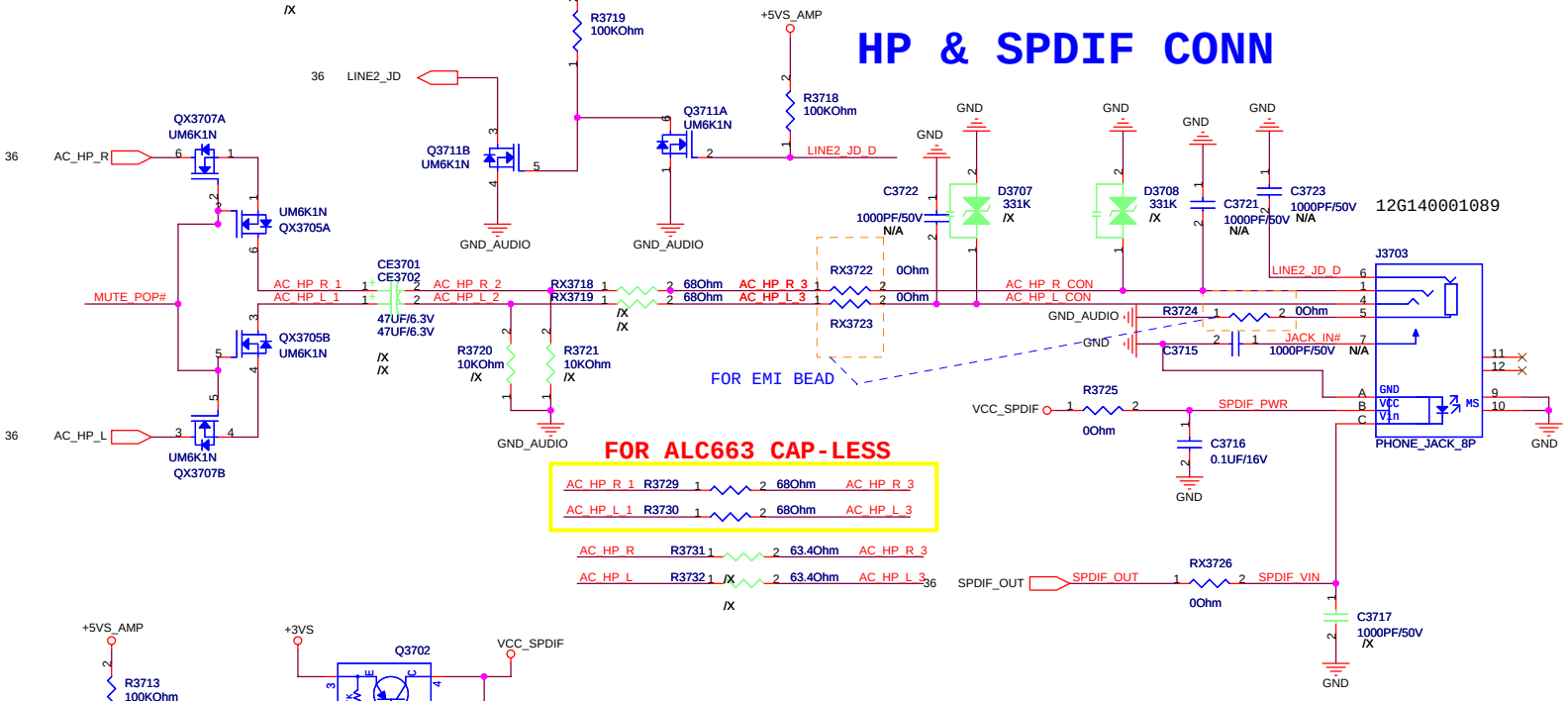




SPEAKER AMP

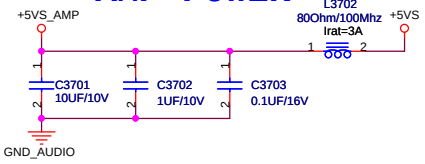


HP & SPDIF CONN

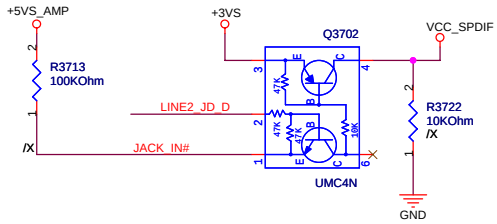


GAIN0	GAIN1	Av(inv)
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB

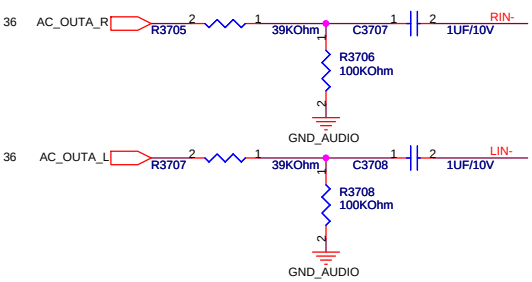
AMP POWER



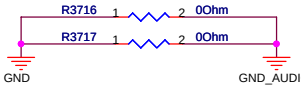
FOR ALC663 CAP-LESS

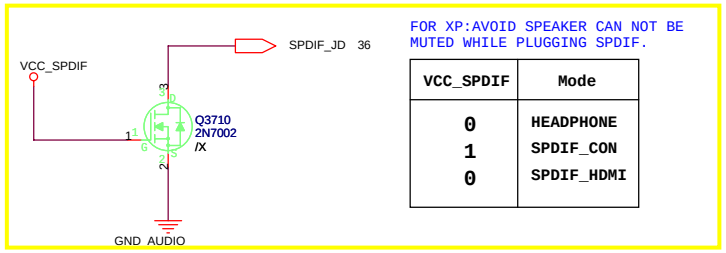


JACK_IN#	LINE2_JD_D	Mode
0	1	SPDIF_CON
0	0	HEADPHONE,SPDIF_HDMI
1	1	SPDIF_HDMI



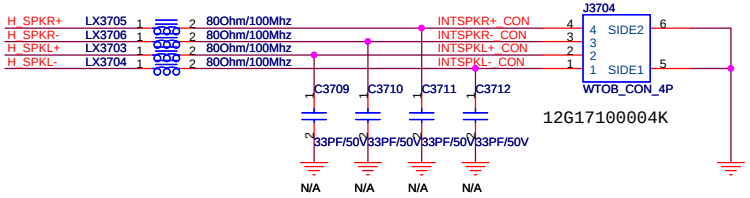
JACK GND

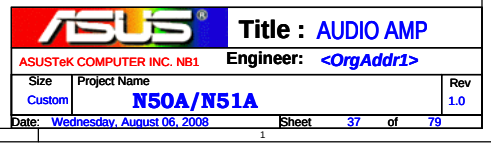




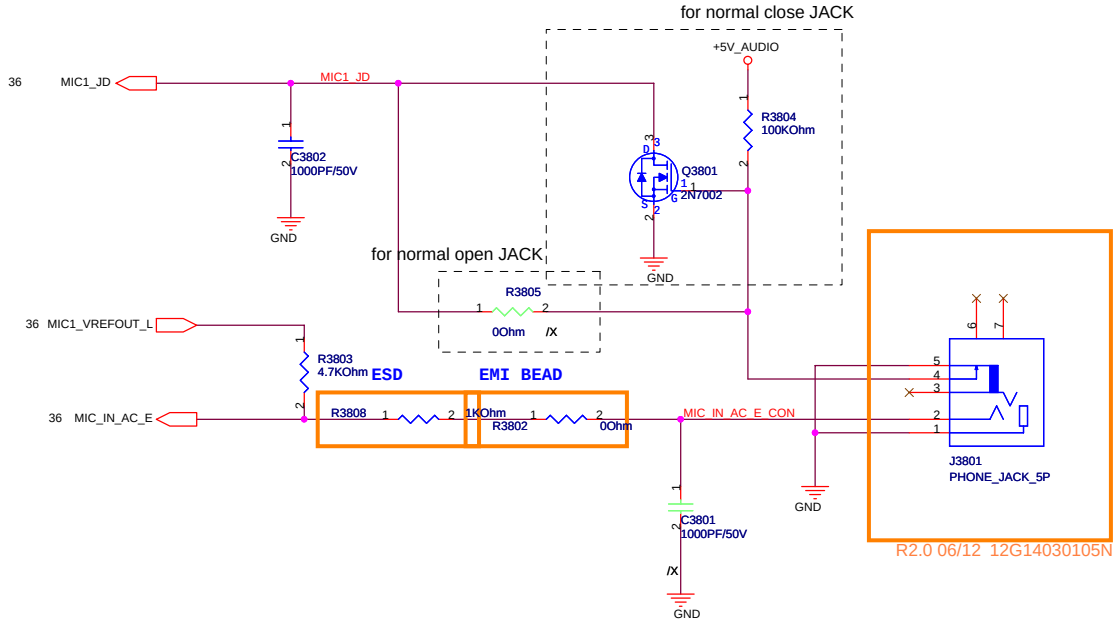
VCC_SPDIF	Mode
0	HEADPHONE
1	SPDIF_CON
0	SPDIF_HDMI

SPEAKER CONNECTOR(2W)





EXTERNAL MICROPHONE



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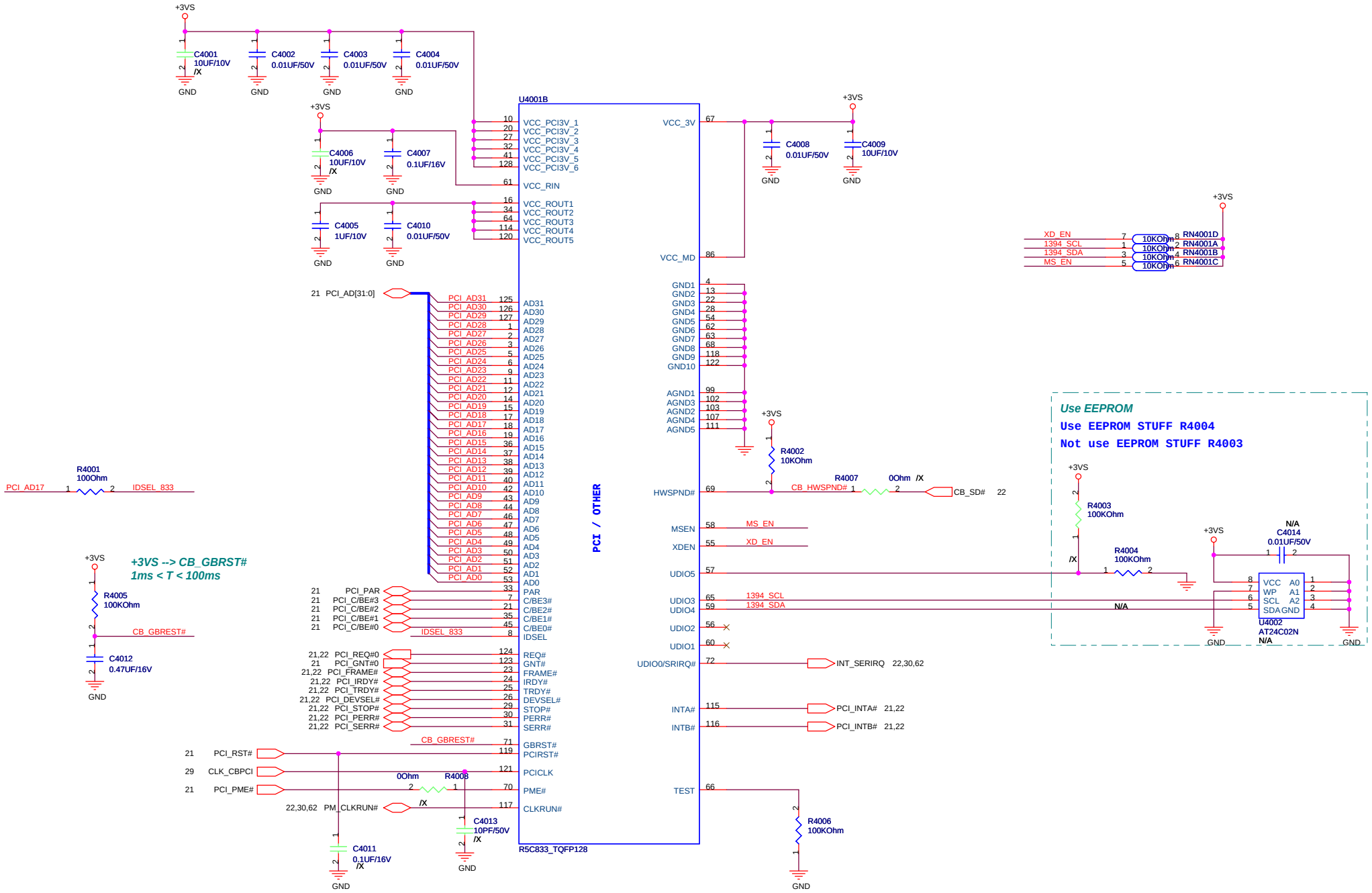
ASUSTeK COMPUTER INC. NB1	Title : MIC&LINEIN	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50A/N51A	Rev: 1.0
Date: Friday, August 01, 2008	Sheet 38 of 79	

ASUSTeK COMPUTER INC. NB1	Title : DSP		
	Engineer: <OrgAddr1>		
Size: A	Project Name: N50A/N51A		Rev: 1.0
Date: Thursday, July 24, 2008	Sheet 39 of 79		



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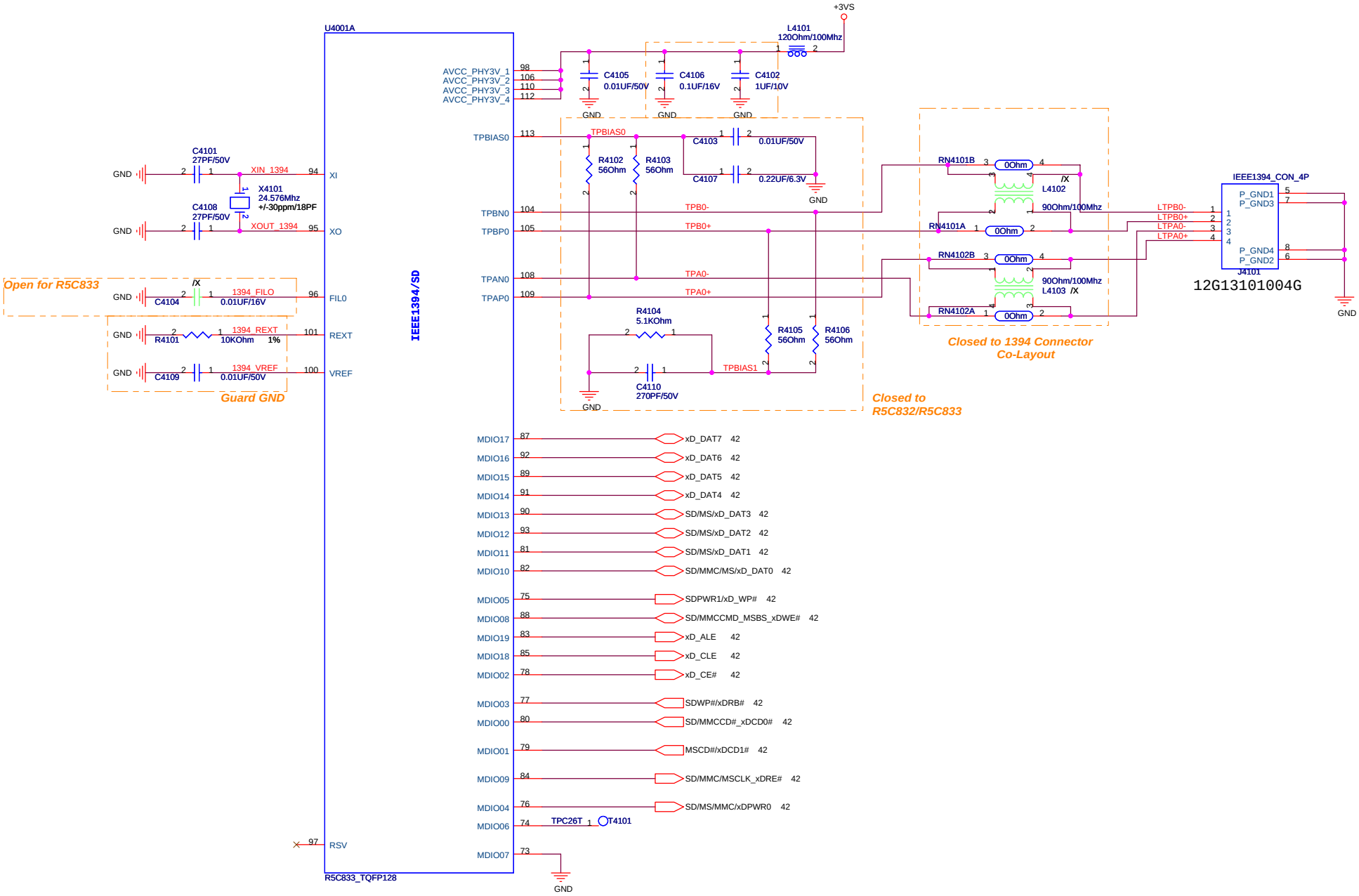
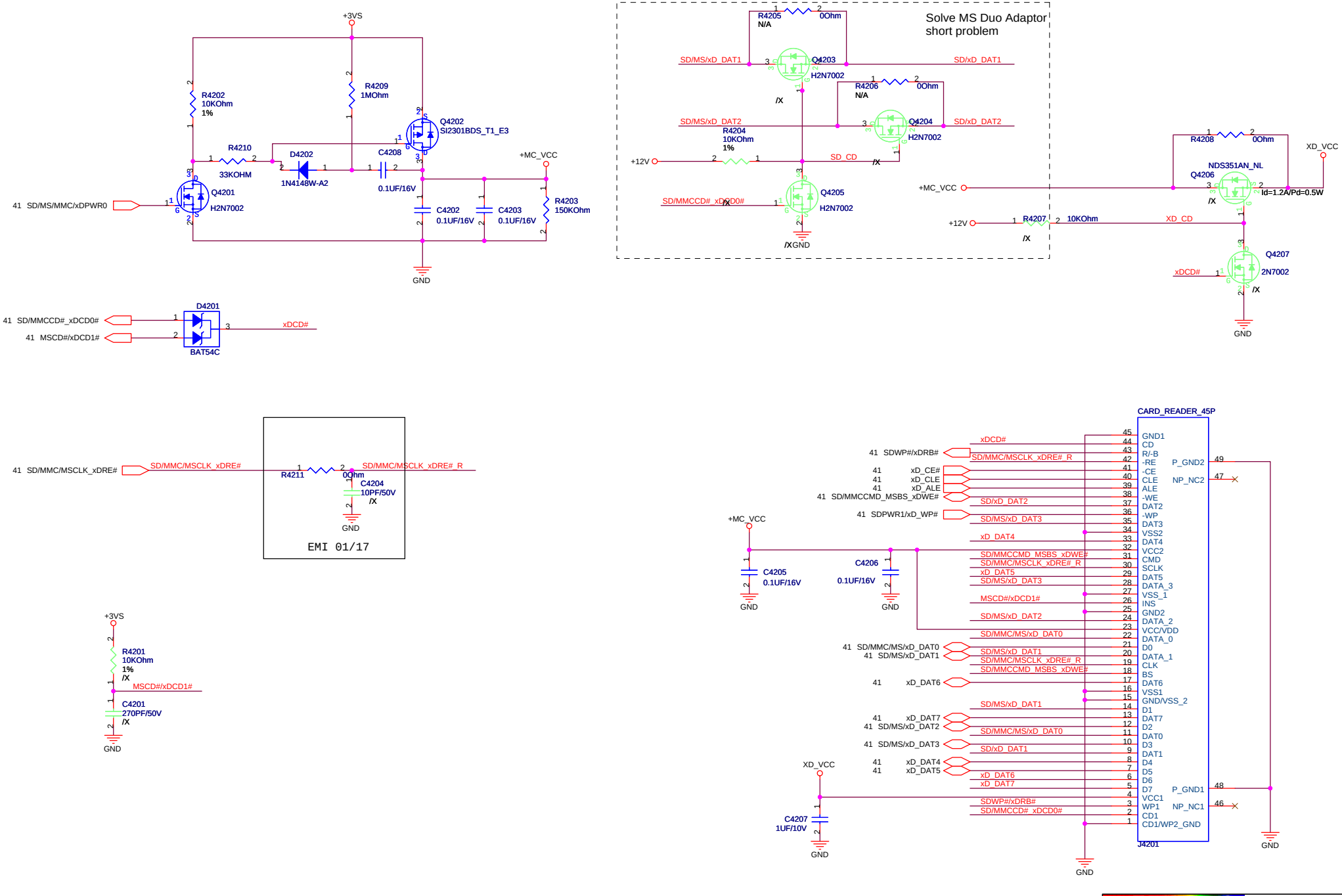
ASUSTeK COMPUTER INC. NB1	Title : CARDBUS R5C833 (1)	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50A/N51A	Rev: 1.0
Date: Tuesday, August 12, 2008	Sheet 40 of 79	



ASUSTeK COMPUTER INC. NB1	Title : CARDBUS R5C833 (2)	
Engineer: <OrgAddr1>		
Size: Custom	Project Name: N50A/N51A	Rev: 1.0
Date: Thursday, August 07, 2008	Sheet 41 of 79	



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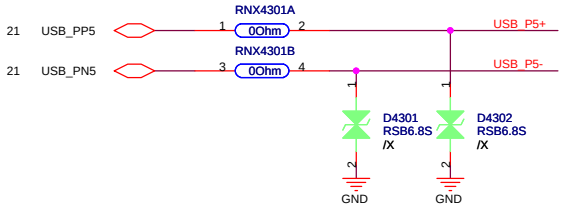
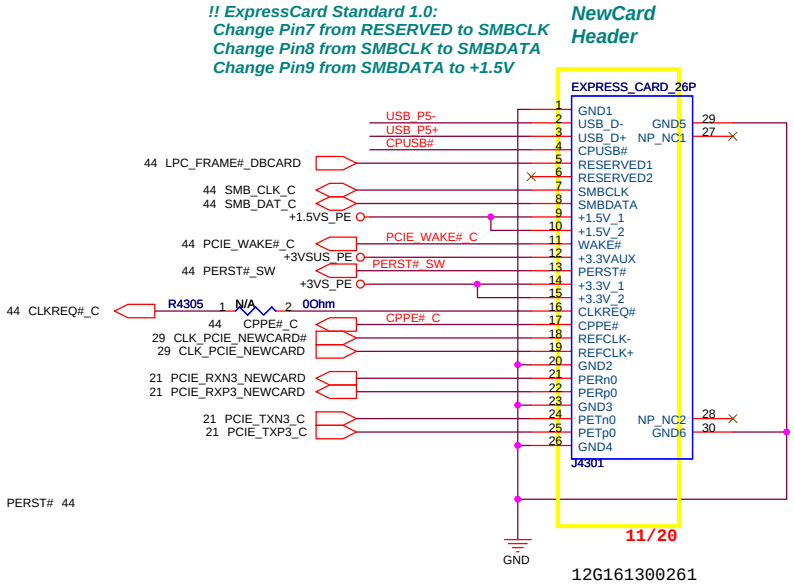
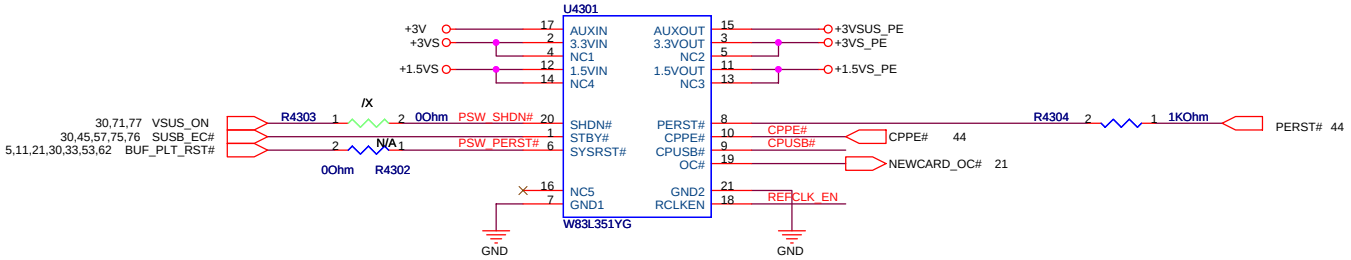
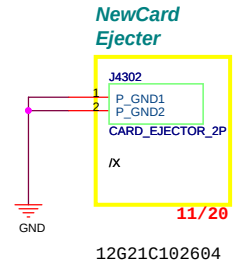
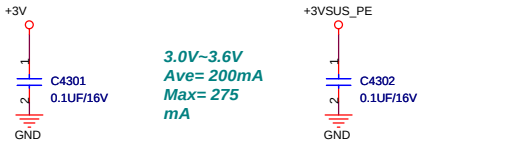


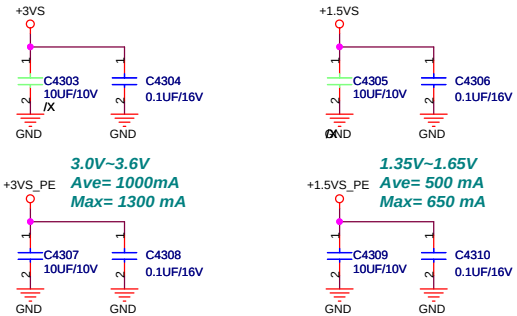


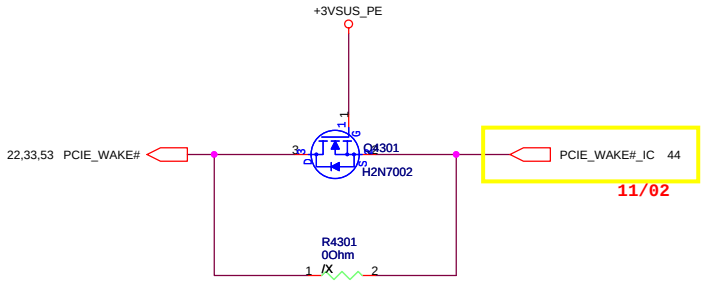
1st source:06G030091010

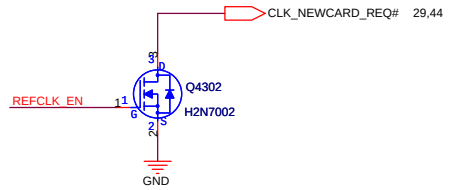






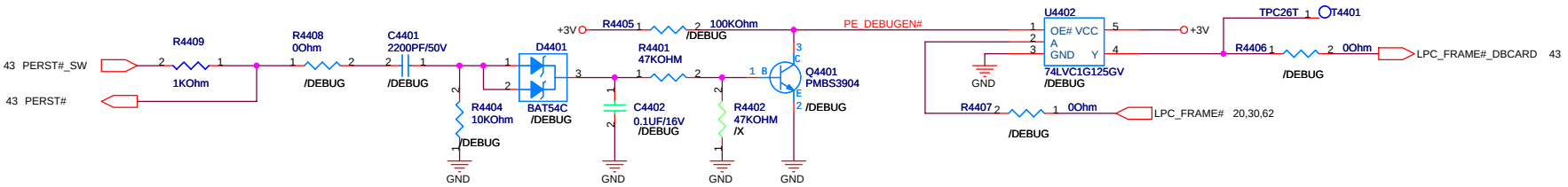


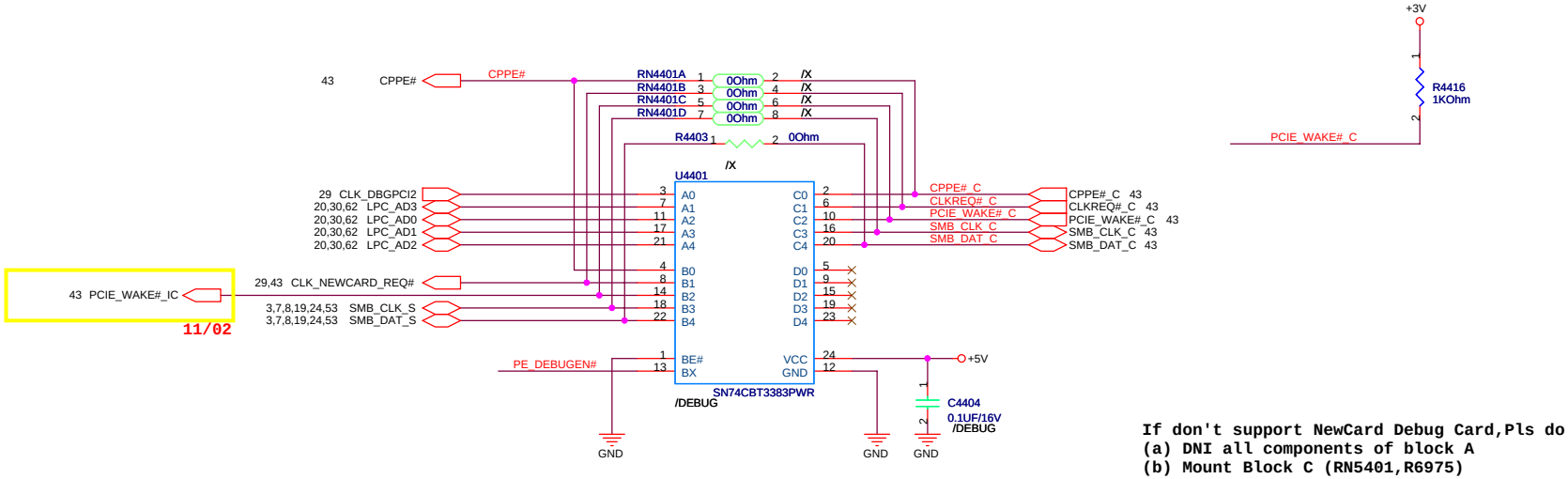




ASUSTeK COMPUTER INC. NB1	Title : NEW CARD	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50A/N51A	Rev: 1.0
Date: Wednesday, August 06, 2008	Sheet 43 of 79	

Block A

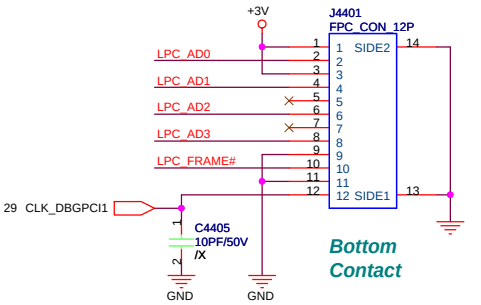


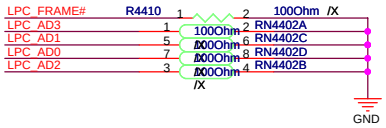


If don't support NewCard Debug Card,Pls do
(a) DNI all components of block A
(b) Mount Block C (RN5401,R6975)

For PCMCIA Debug Card

If support NewCard Debug Card,
Pls don't mount all components.





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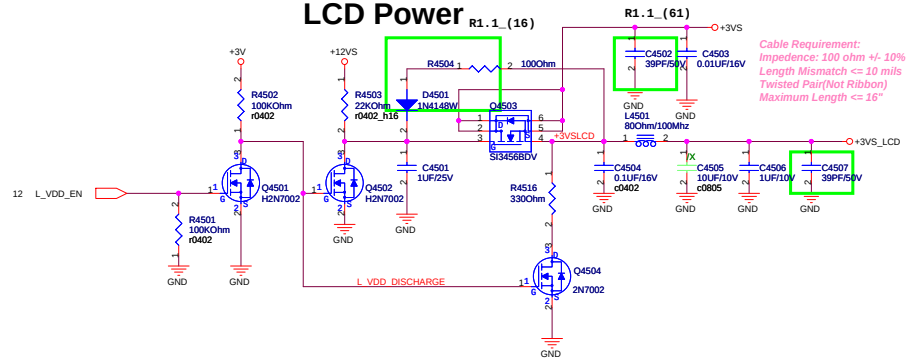
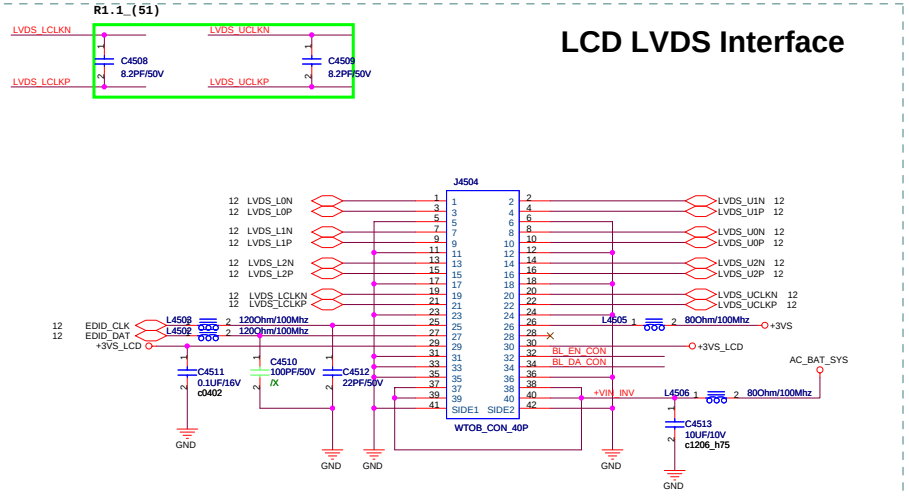
ASUSTeK COMPUTER INC. NB1	Title : DEBUG	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50A/N51A	Rev: 1.0
Date: Monday, August 04, 2008	Sheet 44 of 79	

LCD Backlight Control

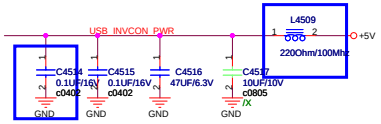
LCD Power

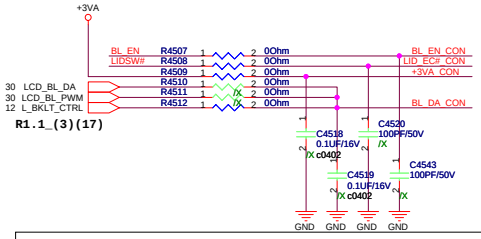


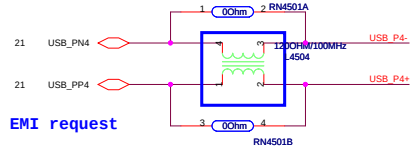
LCD LVDS Interface



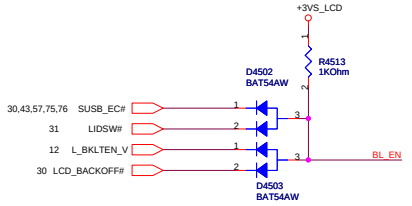
Inverter Interface/Speaker CONN.

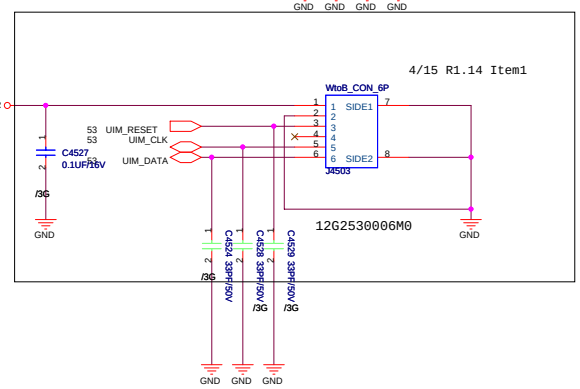


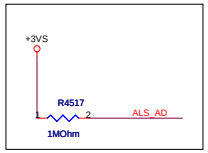


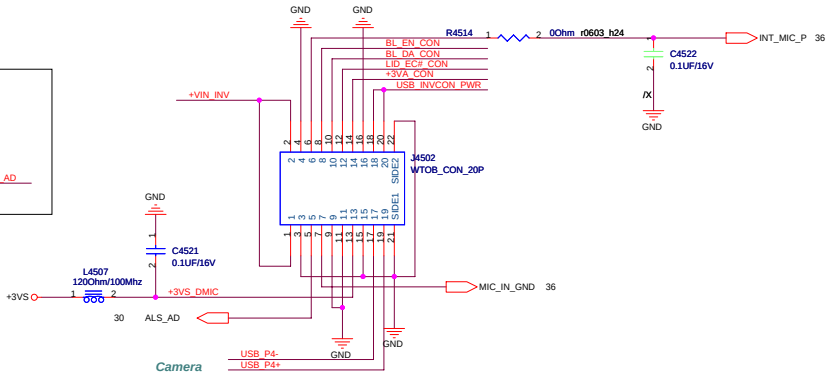


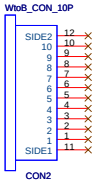
R1.1_(59) change for EMI request











ASUSTeK COMPUTER INC. NB1	Title : LVDS	
	Engineer: <OrgAddr1>	
Size: C	Project Name: N50A/N51A	Rev: 1.0
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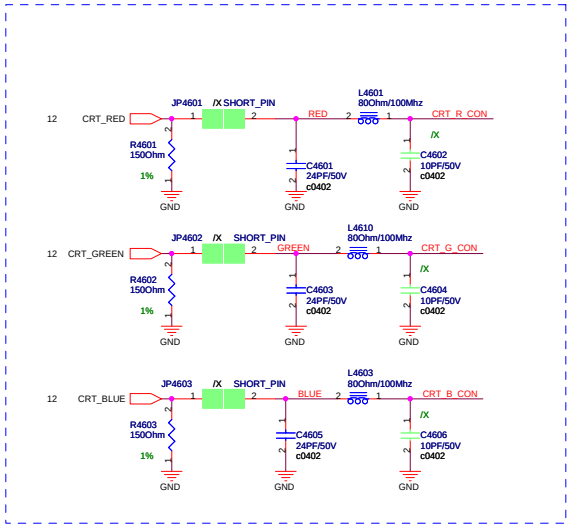
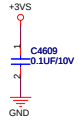
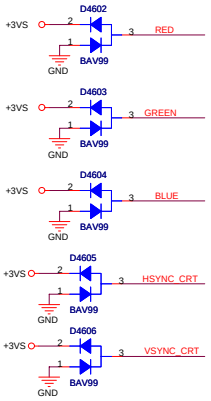
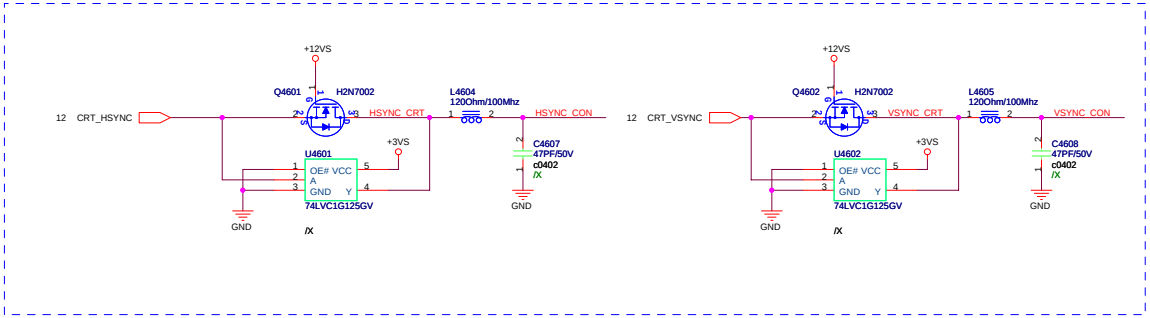


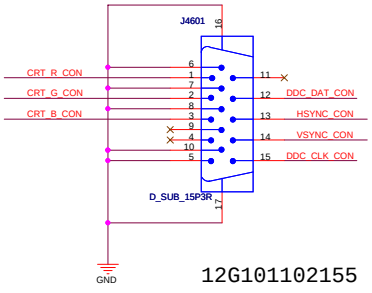


Place a 0.1uF CAP across the ESD Diode close

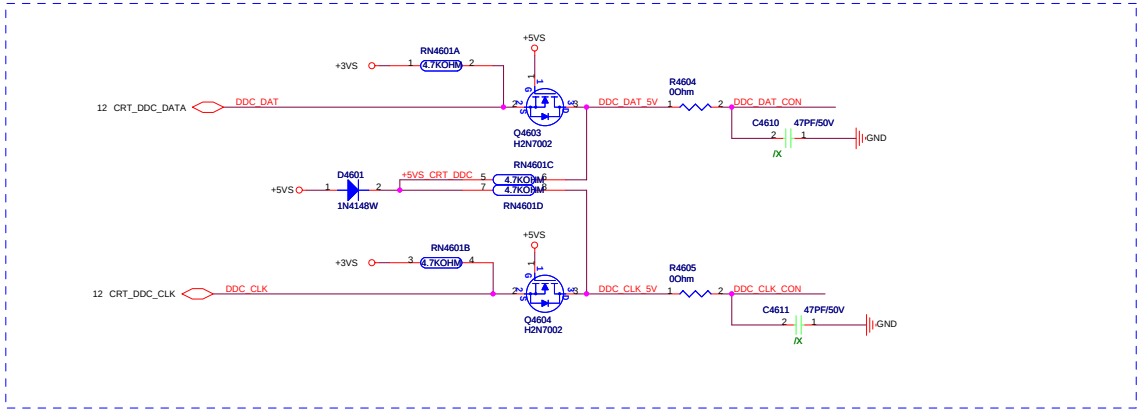


PLACE ESD Diodes near VGA port





12G101102155



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ASUSTeK COMPUTER INC. NB1	Title : CRT	
	Engineer: <OrgAddr1>	
Size: C	Project Name: N50A/N51A	Rev: 1.0
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Title : DVI	
ASUSTeK COMPUTER INC. NB1	Engineer: <OrgAddr1>
Size: A	Project Name: N50A/N51A
Rev: 1.0	
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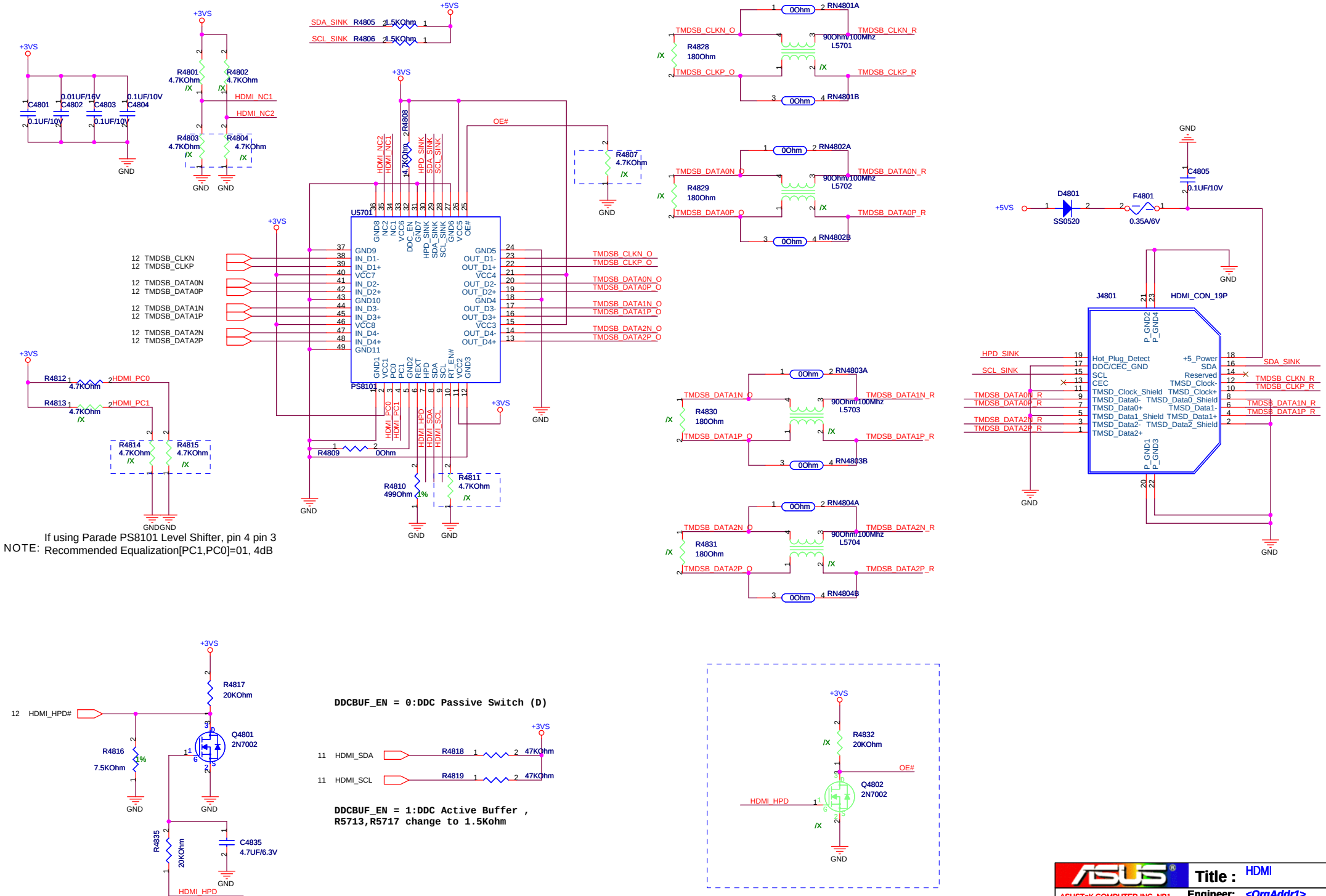

NOTE: If using Parade PS8101 Level Shifter, pin 4 pin 3
Recommended Equalization[PC1,PC0]=01, 4dB

DDCBUF_EN = 0:DDC Passive Switch (D)

DDCBUF_EN = 1:DDC Active Buffer ,
R5713,R5717 change to 1.5Kohm

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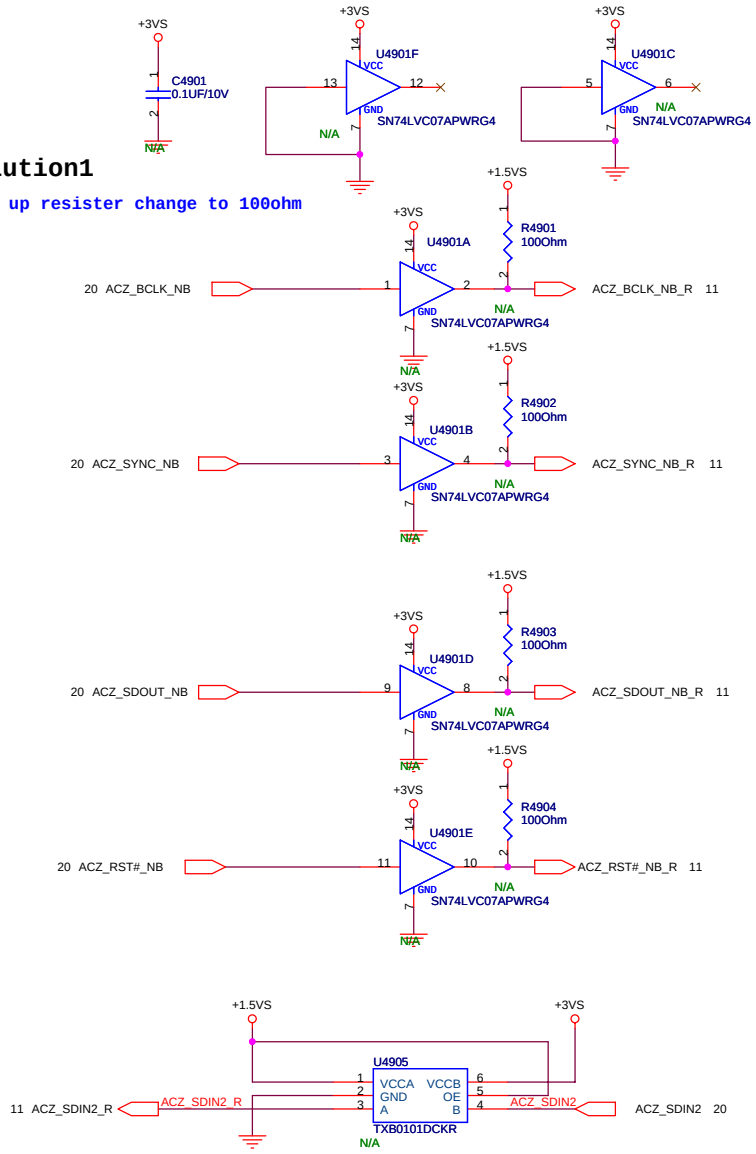
ASUSTeK COMPUTER INC. NB1	Title : HDMI	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50A/N51A	Rev: 1.0
Date: Friday, August 01, 2008	Sheet 48 of 79	

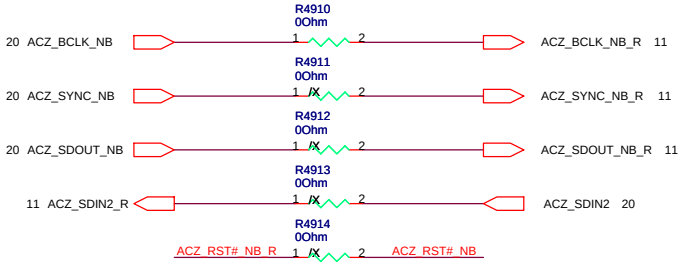
Solution1

pull up resister change to 100ohm



Solution2

for 1.5V HDA



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ASUSTeK COMPUTER INC. NB1

Title :

Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	N50A/N51A	1.0

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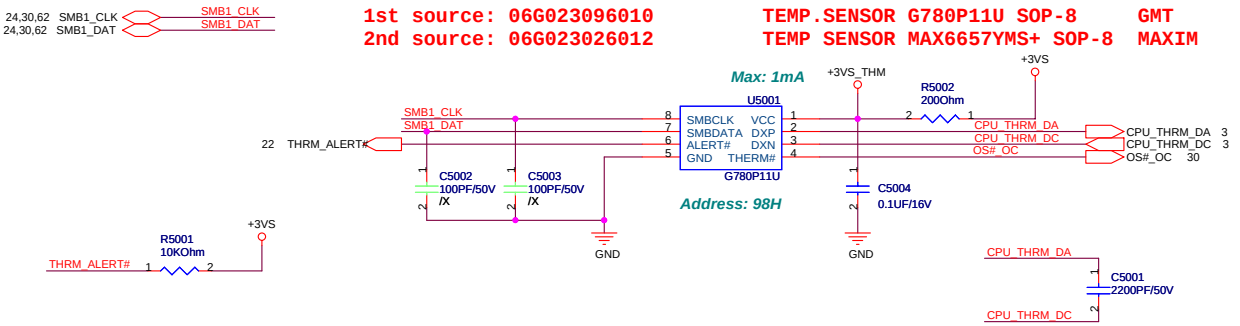
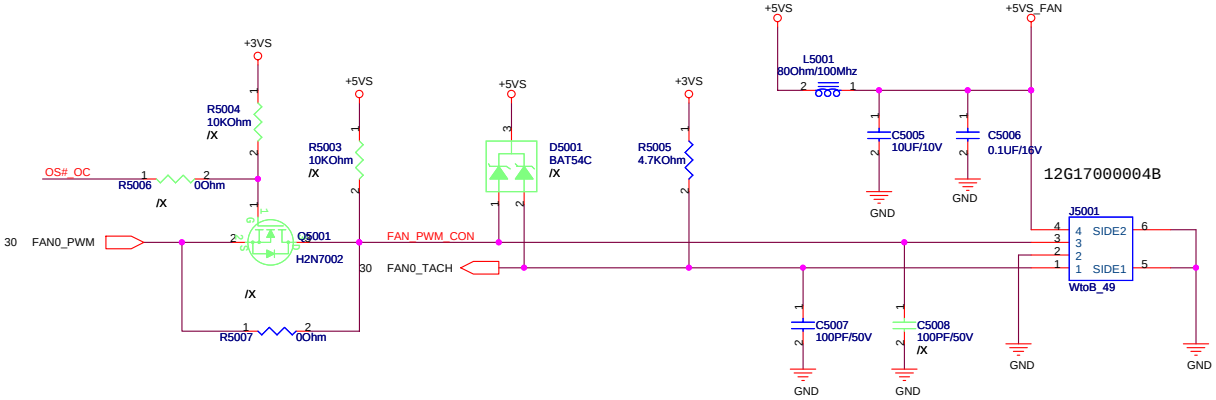
Thermal Sensor



DC FAN Control



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ASUSTeK COMPUTER INC. NB1	Title : Thermal & Fan	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50A/N51A	Rev: 1.0
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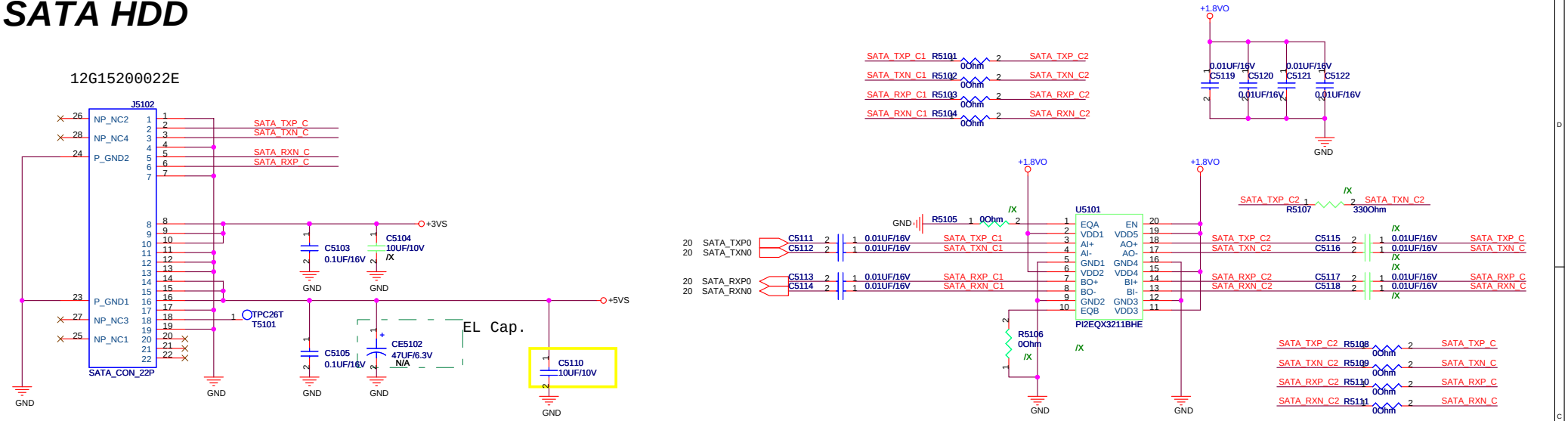
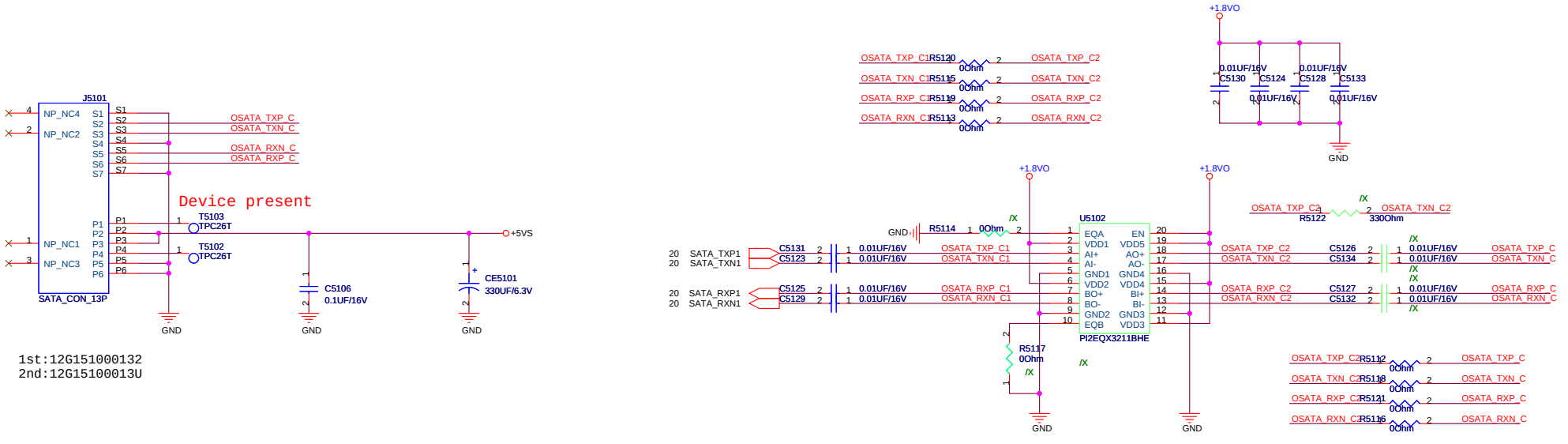
SATA HDD



ODD



ASUSTeK COMPUTER INC. NB1	Title : HDD & CD-ROM	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50A/N51A	Rev: 1.0
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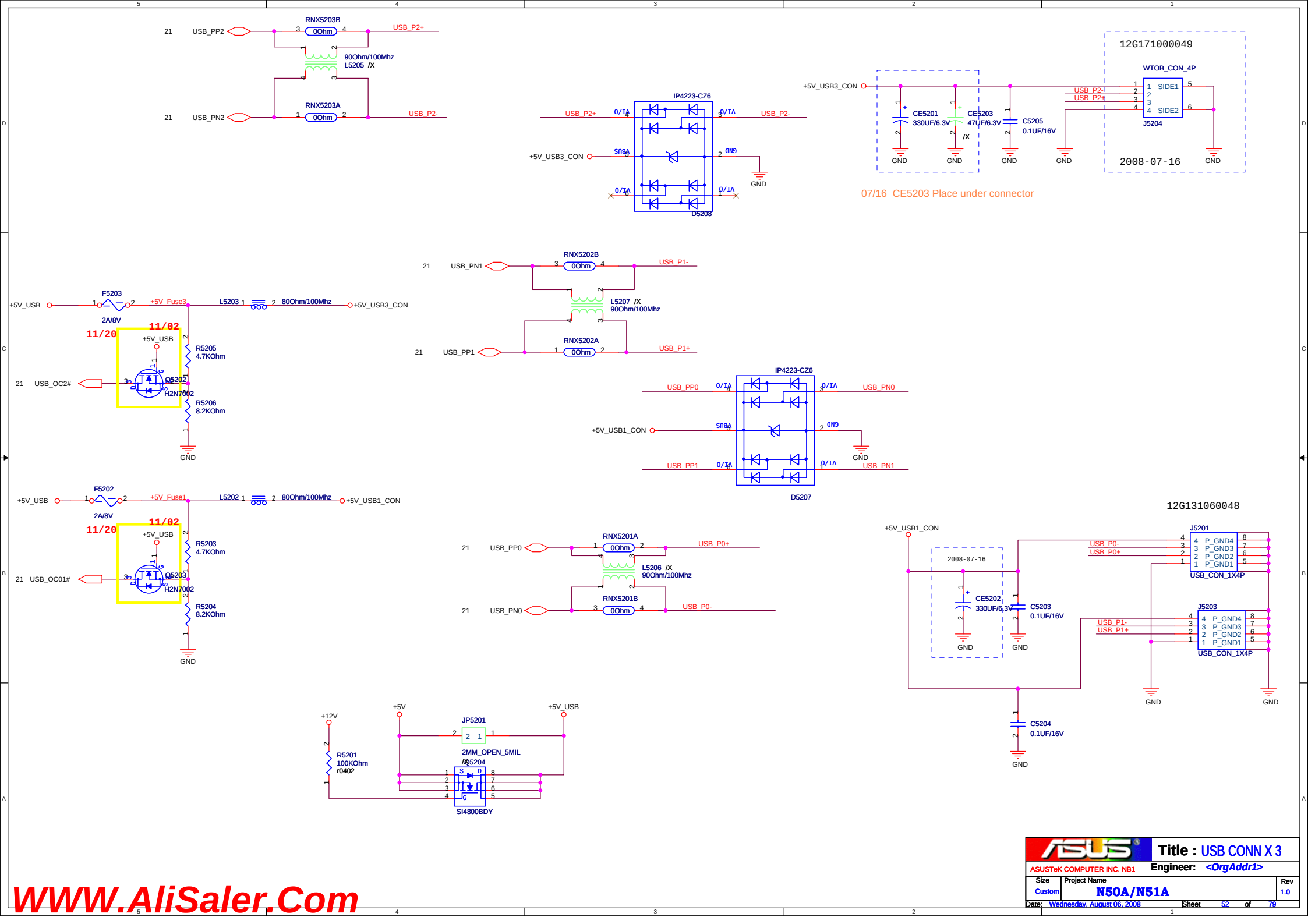

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Title :	USB CONN X 3
ASUSTeK COMPUTER INC. NB1	Engineer: <OrgAddr1>
Size: Custom	Project Name: N50A/N51A
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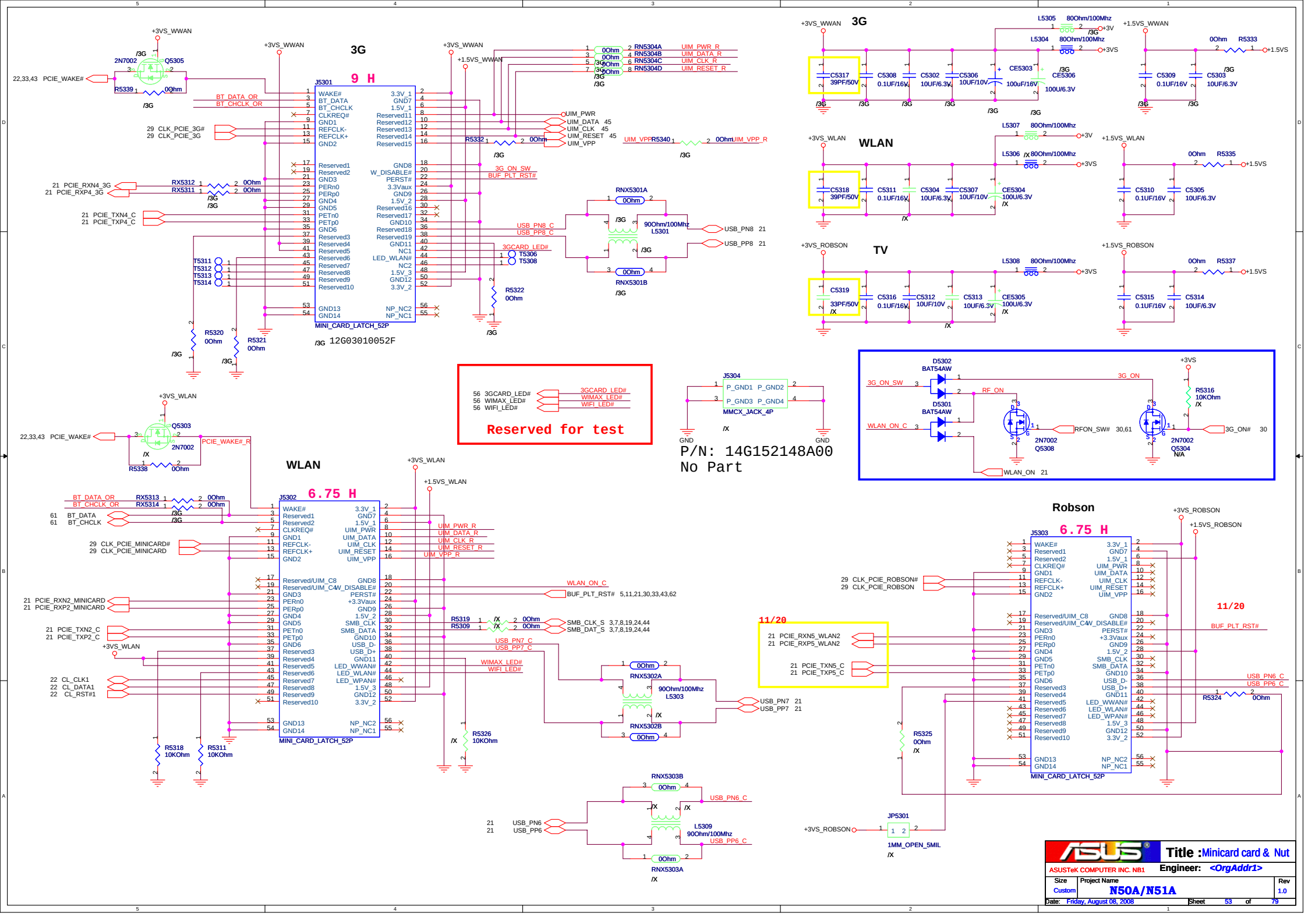
Date: Wednesday, August 06, 2008	Sheet 52 of 79


3G
J5301
9 H
MINI_CARD_LATCH_52P
12G03010052F
WLAN
J5302
6.75 H
MINI_CARD_LATCH_52P
Reserved for test
P/N: 14G152148A00
No Part
Robson
J5303
6.75 H
MINI_CARD_LATCH_52P
11/20
TV
WLAN
3G
Title :Minicard card & Nut
ASUSTeK COMPUTER INC. NB1
Engineer: <OrgAddr1>
Project Name
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ASUSTeK COMPUTER INC. NB1	Title : Port Docking		
	Engineer: <OrgAddr1>		
Size: A	Project Name: N50A/N51A		Rev: 1.0
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Title :	Super I/O & FIR
ASUSTeK COMPUTER INC. NB1	Engineer: <OrgAddr1>
Size: A	Project Name: N50A/N51A
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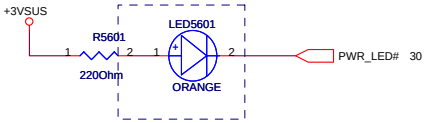
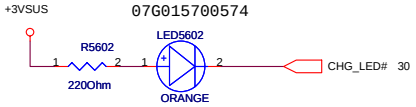
Date: Thursday, July 24, 2008	Sheet 55 of 79

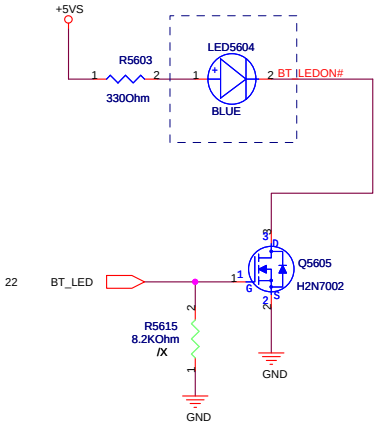
For Power LED



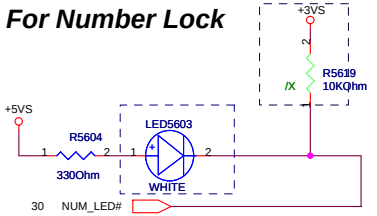
For Battery LED



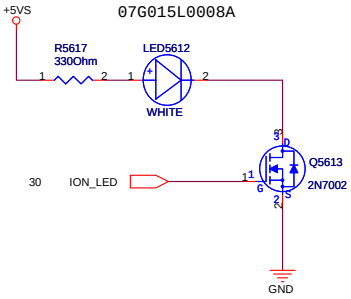
For BT LED



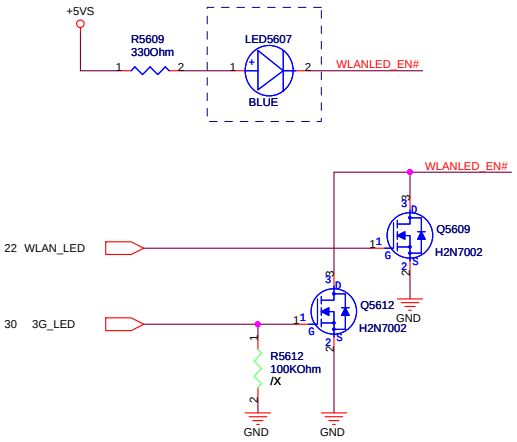
For Number Lock



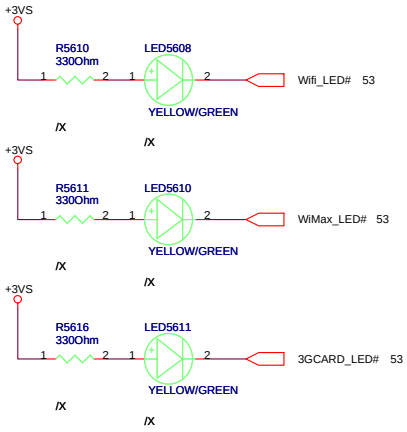
For Ionizer



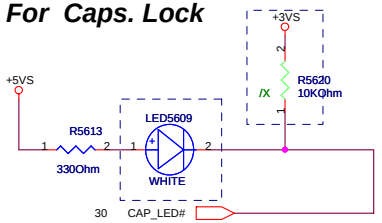
For WireLess LED



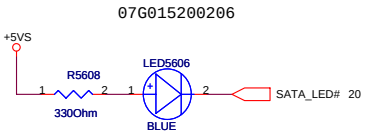
LEDs for testing

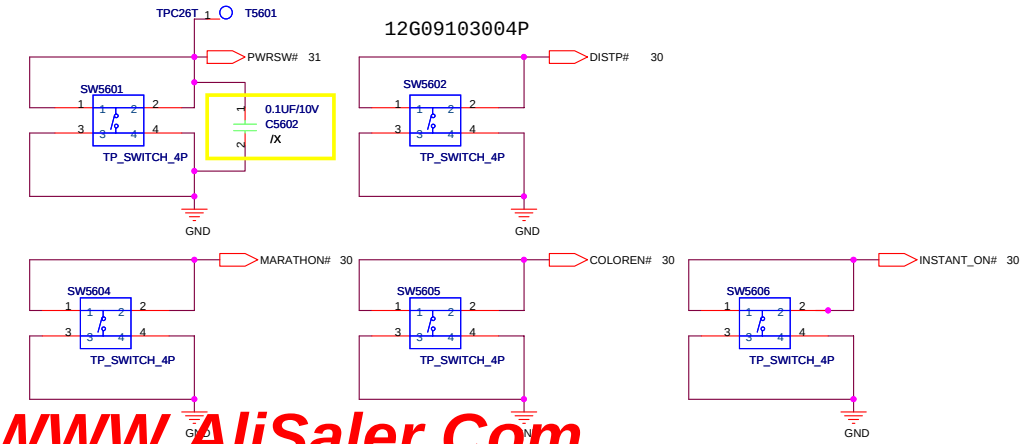


For Caps. Lock

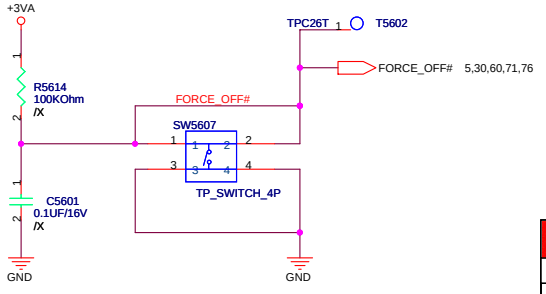


For SATA/IDE LED





SHUT_DOWN#



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ASUSTeK COMPUTER INC. NB1	Title : LED/TP/SW	
	Engineer: <OrgAddr1>	
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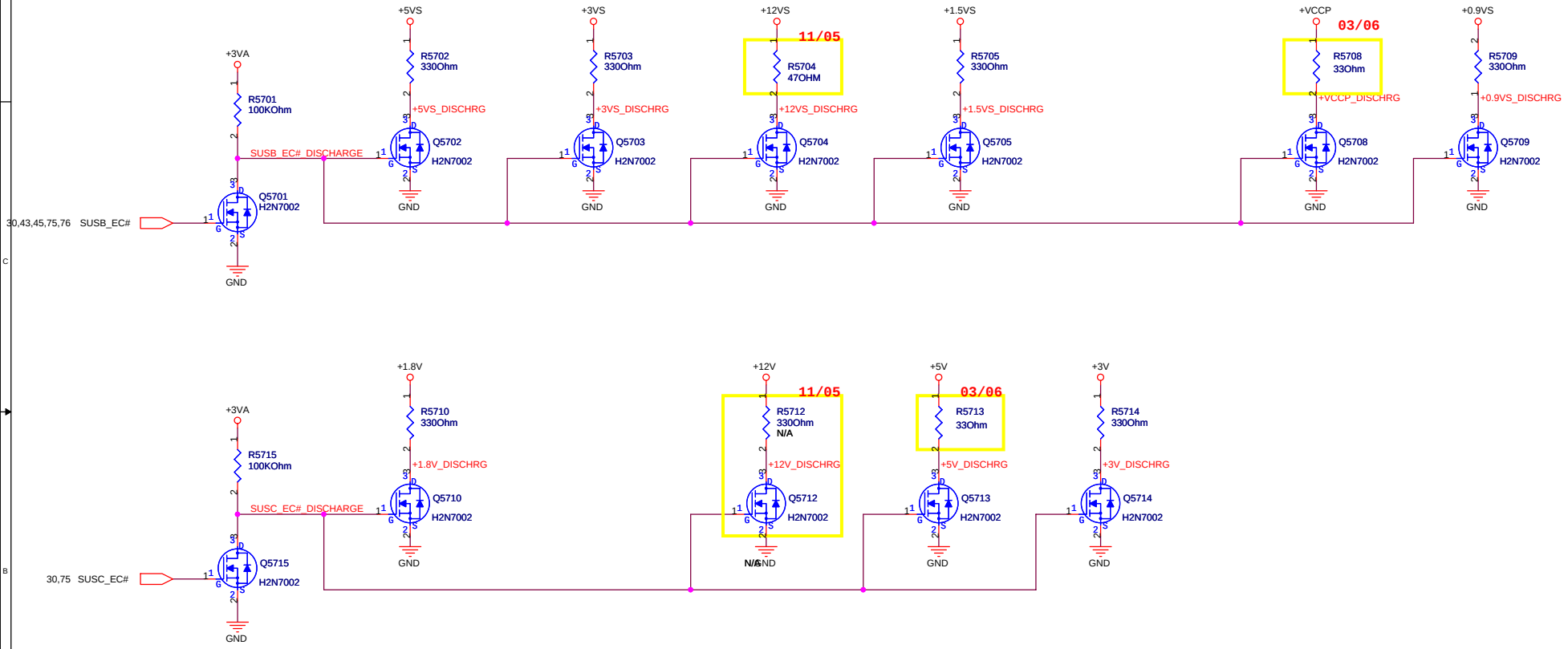

ASUSTeK COMPUTER INC. NB1	Title : DISCHARGE	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50A/N51A	Rev: 1.0
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Title : UWB Minicard card

ASUSTeK COMPUTER INC. NB1

Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	N50A/N51A	1.0

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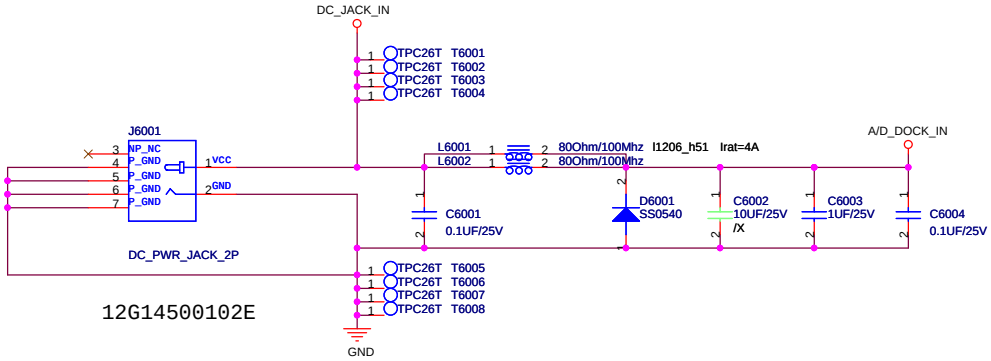
Title :	
ASUSTeK COMPUTER INC. NB1	Engineer: <OrgAddr1>
Size: A	Project Name: N50A/N51A
Rev: 1.0	
Date: Thursday, July 24, 2008	Sheet 59 of 79

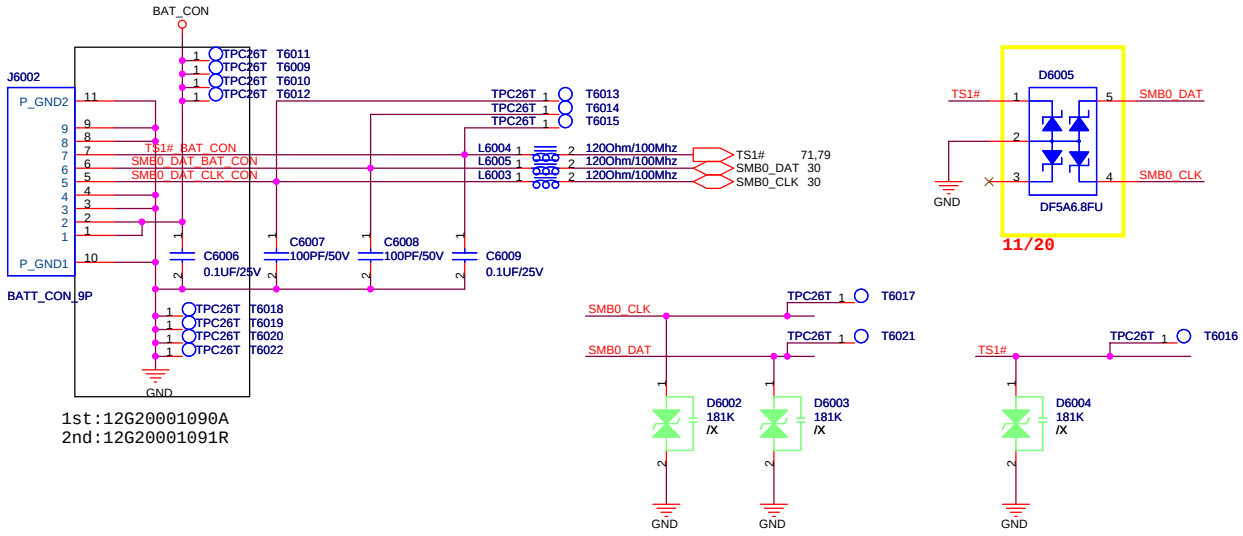
DC IN



12G14500102E

BAT IN

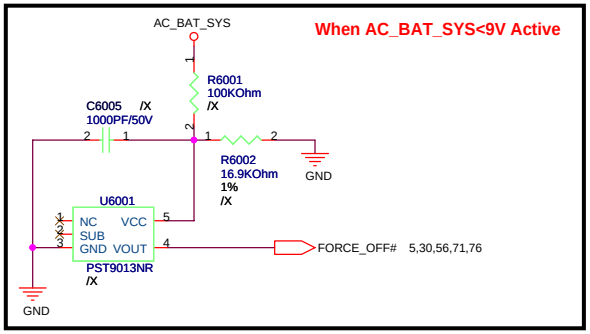
3/11 Pin define follow Battery protection board



1st:12G20001090A
2nd:12G20001091R

11/20

Without Battery & Pull out Adapter



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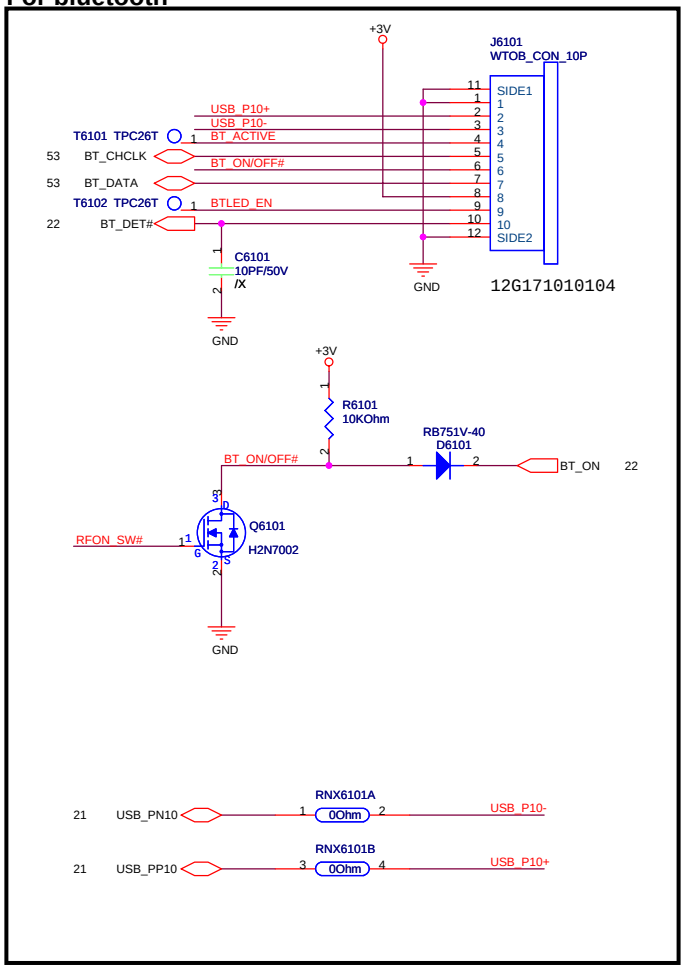
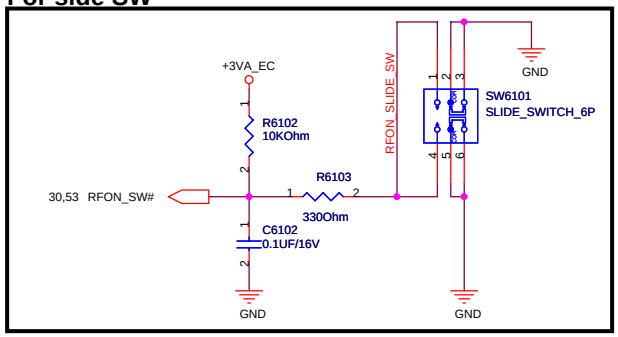
ASUSTeK COMPUTER INC. NB1	Title : DC Jack & Battery CONN	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50A/N51A	Rev: 1.0
Date: Wednesday, August 06, 2008	Sheet 60 of 79	

For bluetooth



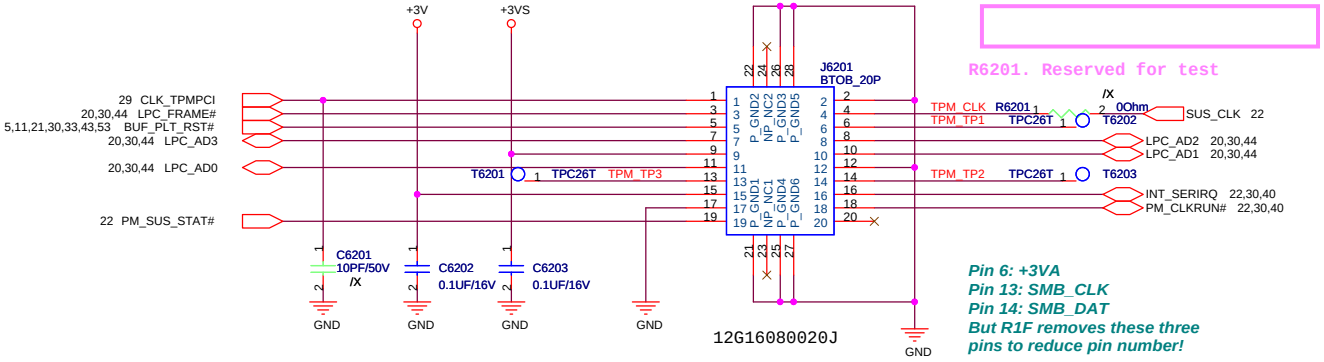
For side SW

12G090070063



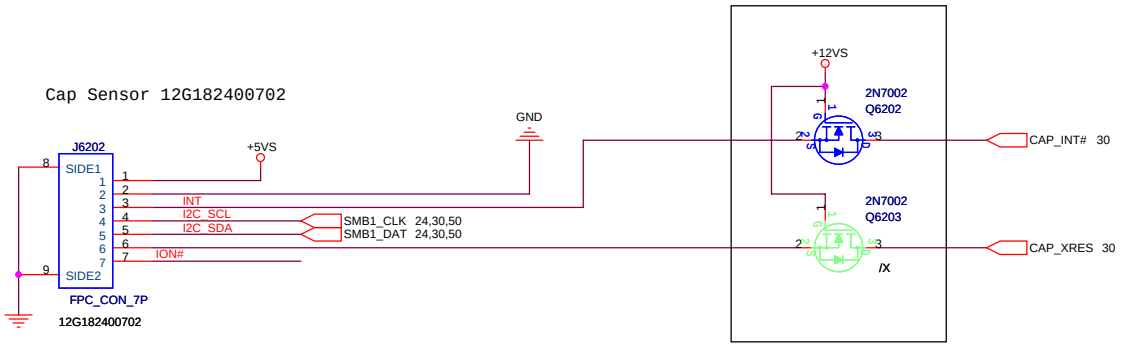
ASUSTeK COMPUTER INC. NB1	Title : BlueTooth	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50A/N51A	Rev: 1.0
Date: Wednesday, August 06, 2008	Sheet 61 of 79	

For TPM module

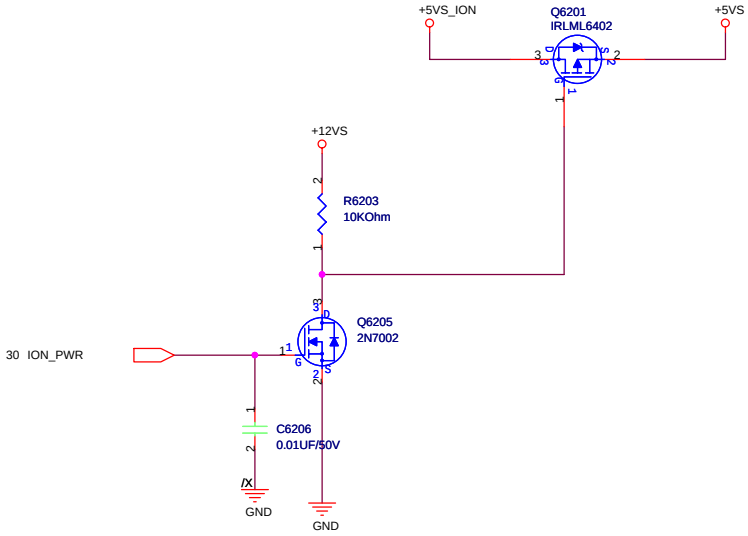


R1.10 04/08 Item1 level shift

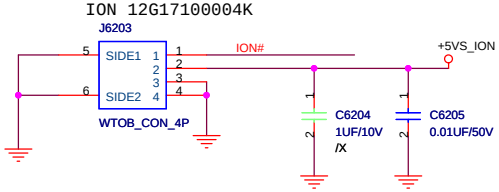
Cap Sensor 12G182400702



R1.10 04/08 Item2 Ion Power control schematic



ION 12G17100004K



ASUSTeK COMPUTER INC. NB1	Title : TPM	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50A/N51A	Rev: 1.0
Date: Wednesday, August 06, 2008	Sheet 62 of 79	

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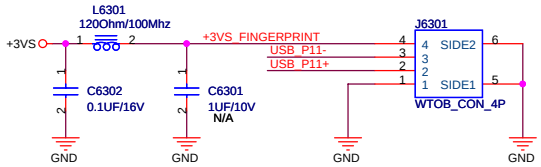

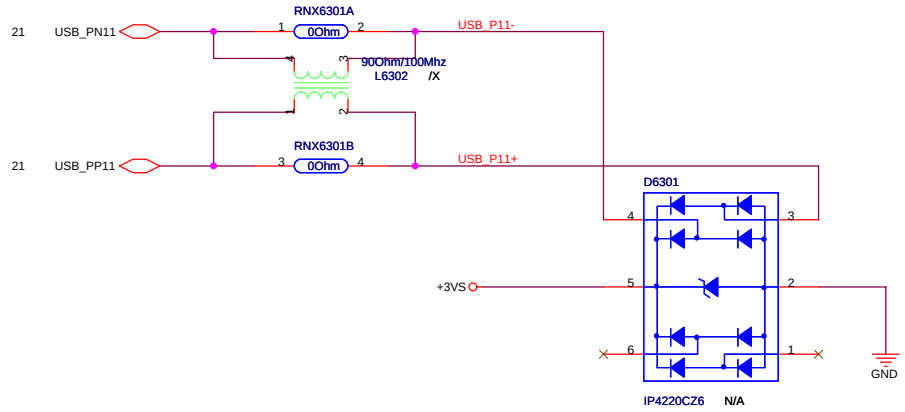

ASUSTeK COMPUTER INC. NB1	Title : Fingerprint		
	Engineer: <OrgAddr1>		
Size: Custom	Project Name: N50A/N51A		Rev: 1.0
Date: Wednesday, August 06, 2008	Sheet 63 of 79		

Title : TUN

ASUSTeK COMPUTER INC. NB1

Engineer: <OrgAddr1>

Size	Project Name	Rev
B	N50A/N51A	1.0

Date: Thursday, July 24, 2008 Sheet 64 of 79

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R1.11 04/10 EMI

U6501 EMI_SPRING_PAD
U6502 EMI_SPRING_PAD
U6503 EMI_SPRING_PAD
/EMI
GND

R2.0 06/18 reserve for EMI

固定孔
H6527
C79D79N
/X

H6524
H6525
H6526
S335D91N
/X
GND

FOR SCREW HOLE

H6501
H6502
H6503
H6514
H6505
H6506
H6507
H6518
H6528
H6509
H6510
H6523
H6511
H6512
H6513
S335D91N
CR226X236D91N
/X
GND

FOR TPM (BOT) 13GN7510M270 FOR MDC (TOP)

H6201
L4E_1A
GND

FOR CPU

H6516
H6520
H6521
H6522
CT268B158D138
/X
GND

13G021029050
FOR 3G (BOT)

H5301
A40M20-64AS
H5302
A40M20-64AS
GND

FOR ROBSON (BOT)

H5303
H5304
CT217B67D47
GND

FOR WLAN (BOT)

13G021043050
FOR UWB (BOT)

H5801
H5802
CT217B67D47
GND

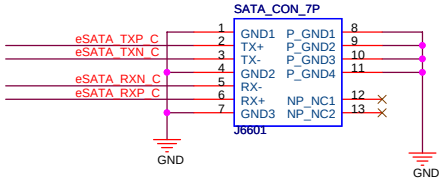
FAN NUT

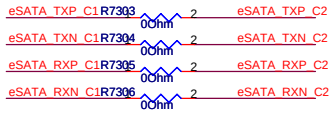
H5306
CT256B315ID146
GND

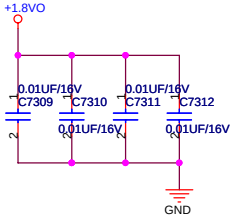
MINI PCI-E CON

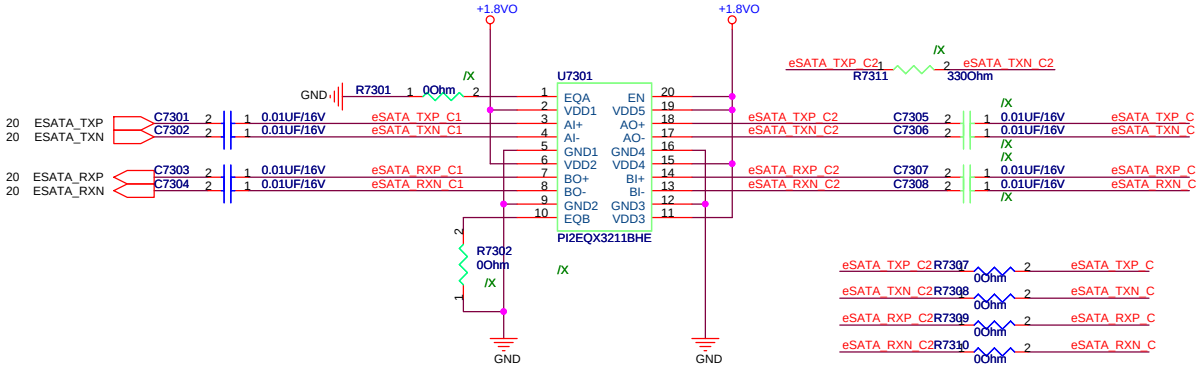
ASUSTeK COMPUTER INC. NB1	Title: MDC NUT & Hinksink NUT	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50A/N51A	Rev: 1.0
Date: Wednesday, August 06, 2008	Sheet 65 of 79	

12G15110007M









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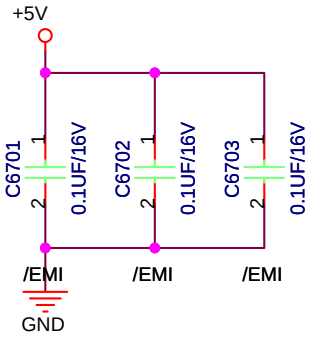
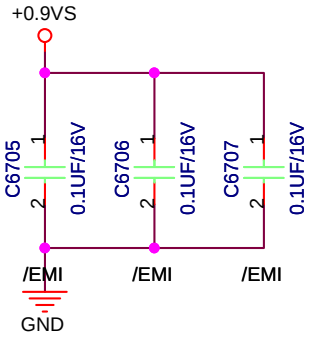
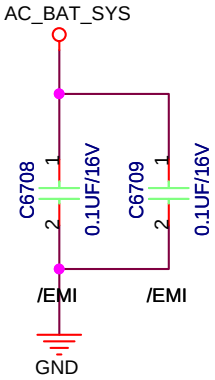
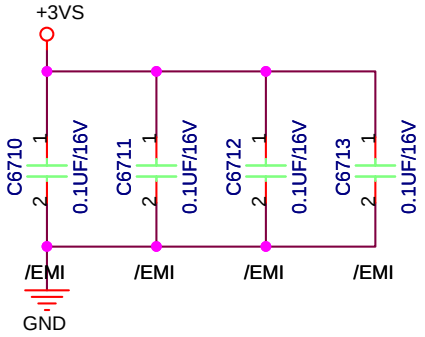
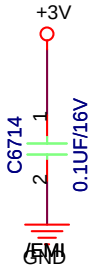
ASUSTeK COMPUTER INC. NB1	Title : E-SATA	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50A/N51A	Rev: 1.0
Date: Friday, August 01, 2008	Sheet 66 of 79	

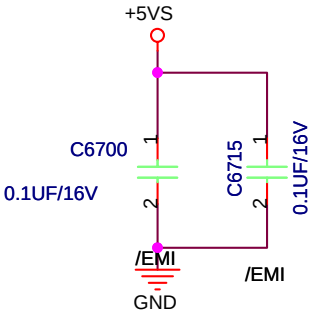


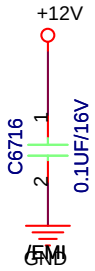












ASUSTeK COMPUTER INC. NB1	Title : Engineer: <OrgAddr1>	
Size: A	Project Name: N50A/N51A	Rev: 1.0
Date: Friday, August 01, 2008	Sheet 67 of 79	

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ASUSTeK COMPUTER INC. NB1	Title : XDP	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: N50A/N51A	Rev: 1.0
Date: Wednesday, August 06, 2008	Sheet 68 of 79	

N50Vm Revision History

Rev	Date	Description
1.0	2007-07-28	Add R4835、C4835 、R2323
	2007/11/22	

Rev	Date	Description

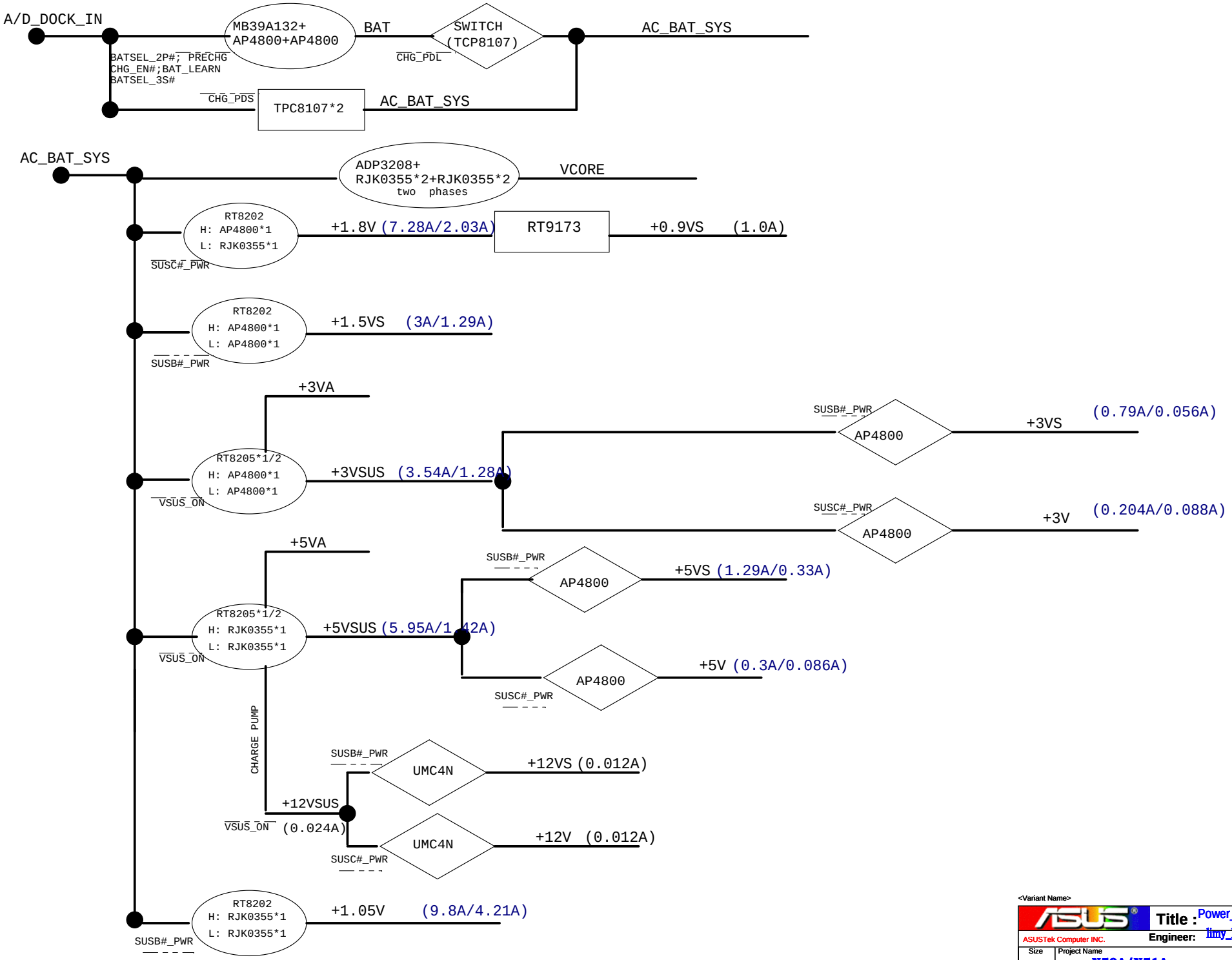
ASUSTeK COMPUTER INC. NB1

Title : HISTORY

Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	N50A/N51A	1.0

Date: Monday, July 28, 2008 Sheet 69 of 79



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<Variant Name>

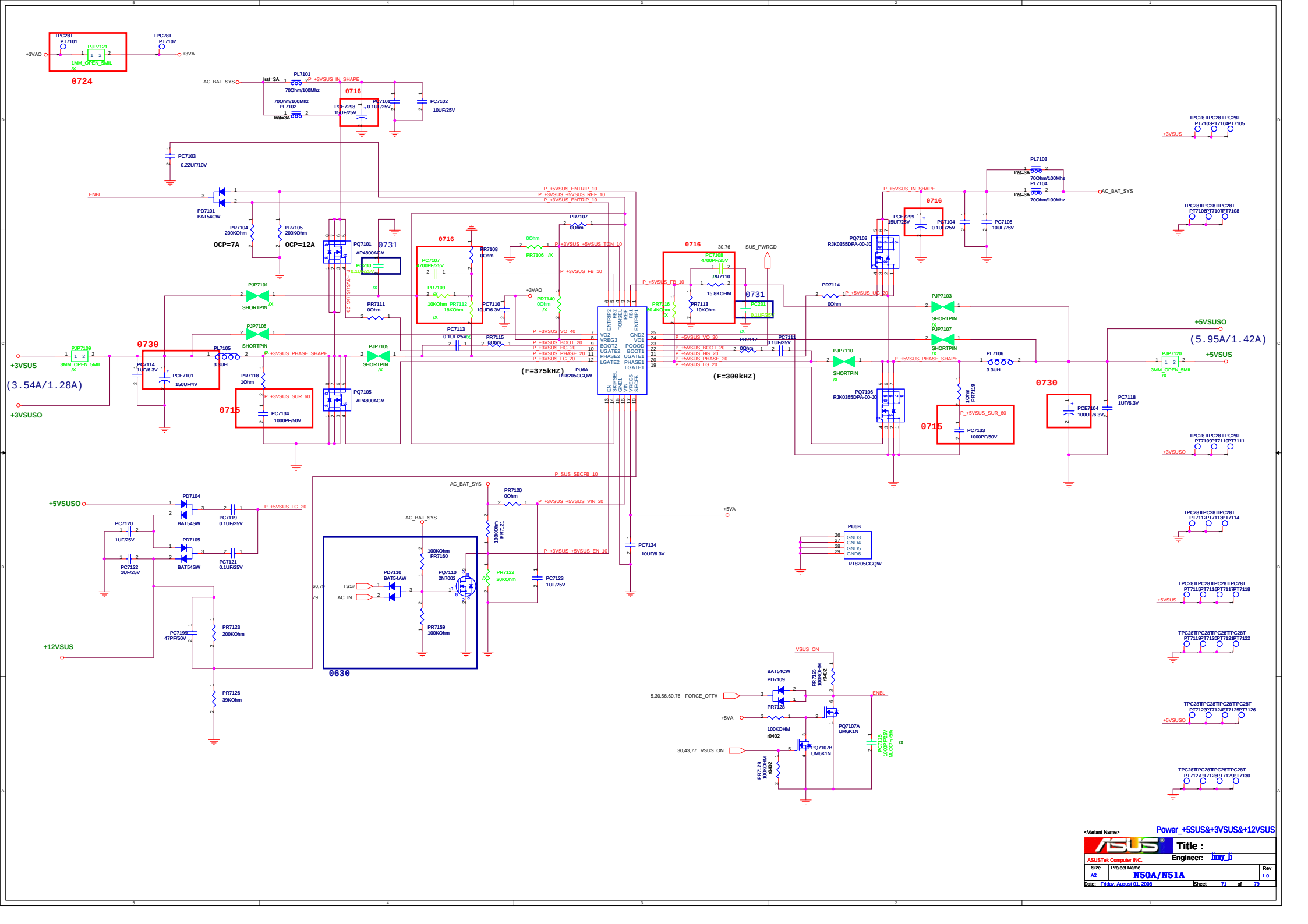
ASUSTek Computer INC.

Title : Power_Flow

Engineer: limy_li

Size	Project Name	Rev
Custom	N50A/N51A	1.0

Date: Friday, August 01, 2008 Sheet 70 of 79


+3VSUS
(3.54A/1.28A)
+3VSUSO
+5VSUSO
(5.95A/1.42A)
+5VSUS
+12VSUS
+3VAO
+5VA
AC_BAT_SYS
ENBL
SUS_PWRGD
VSUS_ON
(F=375kHZ)
(F=300kHZ)
OCP=7A
OCP=12A
0724
0716
0731
0730
0715
0630
PU6A RT8205CGQW
PU6B RT8205CGQW
PQ7103 RJK0355DPA-00-J0
PQ7106 RJK0355DPA-00-J0
PQ7107A UM6K1N
PQ7107B UM6K1N
PQ7110 2N7002
PD7101 BAT54CW
PD7104 BAT54SW
PD7105 BAT54SW
PD7109 BAT54CW
PD7110 BAT54AW
PJP7101 SHORTPIN
PJP7103 SHORTPIN
PJP7105 SHORTPIN
PJP7106 SHORTPIN
PJP7107 SHORTPIN
PJP7110 SHORTPIN
PJP7109 3MM_OPEN_5MIL
PJP7120 3MM_OPEN_5MIL
PJP7121 1MM_OPEN_5MIL
PL7101 70Ohm/100Mhz
PL7102 70Ohm/100Mhz
PL7103 70Ohm/100Mhz
PL7104 70Ohm/100Mhz
PL7105 3.3UH
PL7106 3.3UH
PCE7298 15UF/25V
PCE7299 15UF/25V
PCE7101 150UF/4V
PCE7104 100UF/6.3V
PC7101 0.1UF/25V
PC7102 10UF/25V
PC7103 0.22UF/10V
PC7104 0.1UF/25V
PC7105 10UF/25V
PC7106 4700PF/25V
PC7107 4700PF/25V
PC7108 4700PF/25V
PC7109 0.1UF/25V
PC7110 10UF/6.3V
PC7111 0.1UF/25V
PC7113 0.1UF/25V
PC7114 1UF/6.3V
PC7115 0.1UF/25V
PC7118 1UF/6.3V
PC7119 0.1UF/25V
PC7120 1UF/25V
PC7121 0.1UF/25V
PC7122 1UF/25V
PC7123 1UF/25V
PC7124 10UF/6.3V
PC7125 1000PF/25V
PC7126 47PF/50V
PC7133 1000PF/50V
PC7134 1000PF/50V
PC7230 0.1UF/25V
PC7231 0.1UF/25V
PR7101 0Ohm
PR7104 200KOhm
PR7105 200KOhm
PR7106 0Ohm
PR7107 0Ohm
PR7108 0Ohm
PR7109 10KOhm
PR7110 15.8KOHM
PR7111 0Ohm
PR7112 18KOhm
PR7113 10KOhm
PR7114 0Ohm
PR7115 0Ohm
PR7116 30.4KOhm
PR7117 0Ohm
PR7118 10Ohm
PR7119 10Ohm
PR7120 0Ohm
PR7121 10KOhm
PR7122 20KOhm
PR7123 200KOhm
PR7125 100KOHM
PR7126 39KOhm
PR7127 100KOHM
PR7128 100KOHM
PR7129 10KOHM
PR7140 0Ohm
PR7160 100KOhm
PR7159 100KOhm
PU7101 AP4800AGM
PU7105 AP4800AGM
TPC28T PT7101
TPC28T PT7102
TPC28T PT7103
TPC28T PT7104
TPC28T PT7105
TPC28T PT7106
TPC28T PT7107
TPC28T PT7108
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TPC28T PT7110
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TPC28T PT7112
TPC28T PT7113
TPC28T PT7114
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TPC28T PT7124
TPC28T PT7125
TPC28T PT7126
TPC28T PT7127
TPC28T PT7128
TPC28T PT7129
TPC28T PT7130
P_+5VSUS_ENTRIP_10
P_+3VSUS_+5VSUS_REF_10
P_+3VSUS_ENTRIP_10
P_+3VSUS_+5VSUS_TON_10
P_+3VSUS_FB_10
P_+5VSUS_FB_10
P_+5VSUS_VO_30
P_+3VSUS_VO_40
P_+3VSUS_BOOT_20
P_+5VSUS_BOOT_20
P_+3VSUS_HG_20
P_+5VSUS_HG_20
P_+3VSUS_PHASE_20
P_+5VSUS_PHASE_20
P_+3VSUS_LG_20
P_+5VSUS_LG_20
P_+5VSUS_UG_20
P_+3VSUS_SUR_60
P_+5VSUS_SUR_60
P_SUS_SECFB_10
P_+3VSUS_+5VSUS_VIN_20
P_+3VSUS_+5VSUS_EN_10
P_+5VSUS_IN_SHAPE
P_+3VSUS_PHASE_SHAPE
P_+5VSUS_PHASE_SHAPE
ENTRIP2 FB2 TONSEL REF RB1 ENTRIP1
VO2 VREG3 BOOT2 UGATE2 PHASE2 LGATE2
GND2 VO1 PGOOD BOOT1 UGATE1 PHASE1 LGATE1
EN SKIPSEL SWD1 VIN VREG5 SECFB
GND3 GND4 GND5 GND6
TS1# AC_IN
FORCE_OFF# VSUS_ON
ASUSTek Computer INC.
Title : Power_+5SUS&+3VSUS&+12VSUS
Engineer: Jimy_li
Size A2
Project Name N50A/N51A
Rev 1.0
Date: Friday, August 01, 2008
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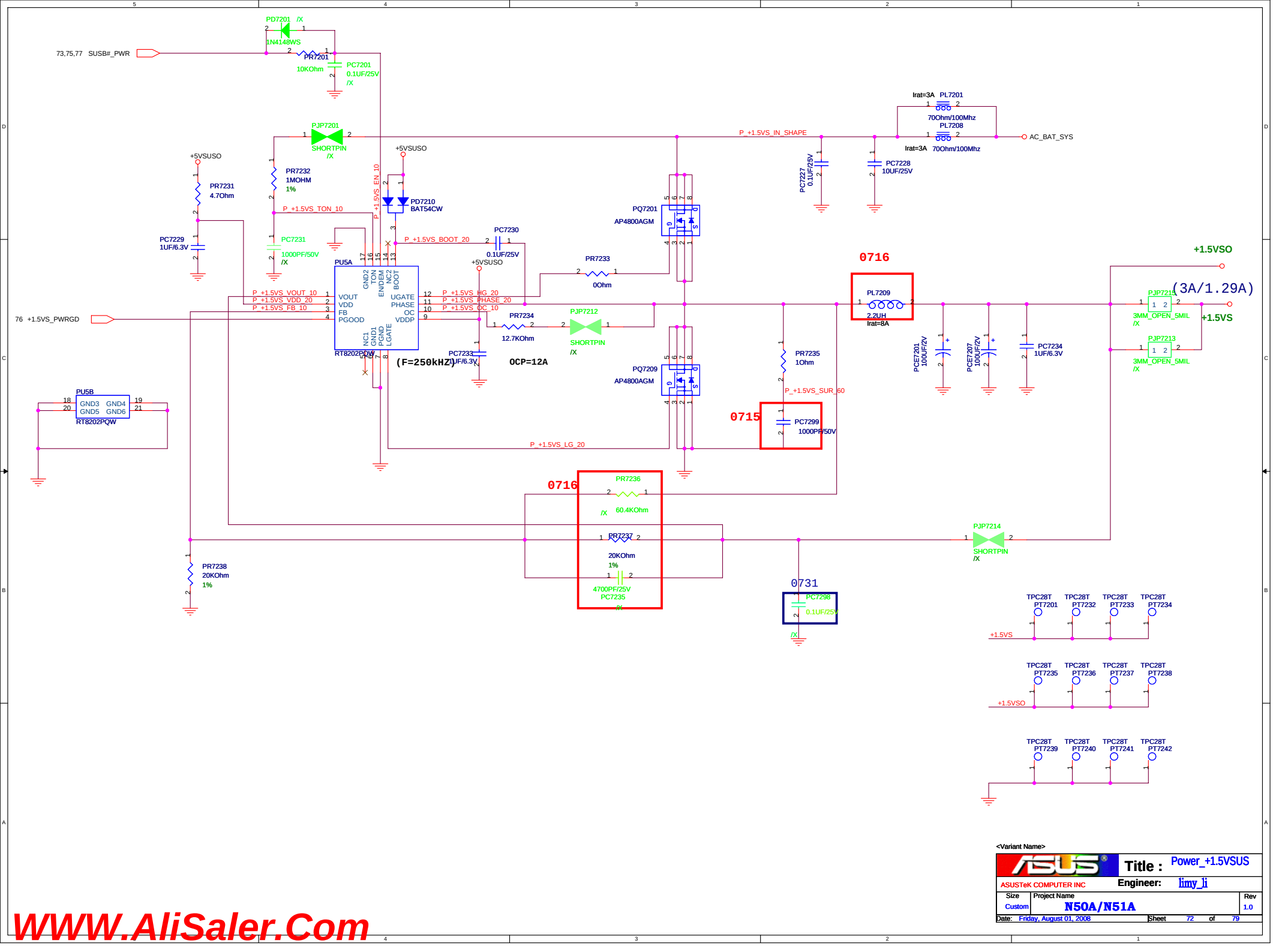

<Variant Name>

ASUSTeK COMPUTER INC

Title : Power_+1.5VSUS

Engineer: limy_li

Size	Project Name	Rev
Custom	N50A/N51A	1.0

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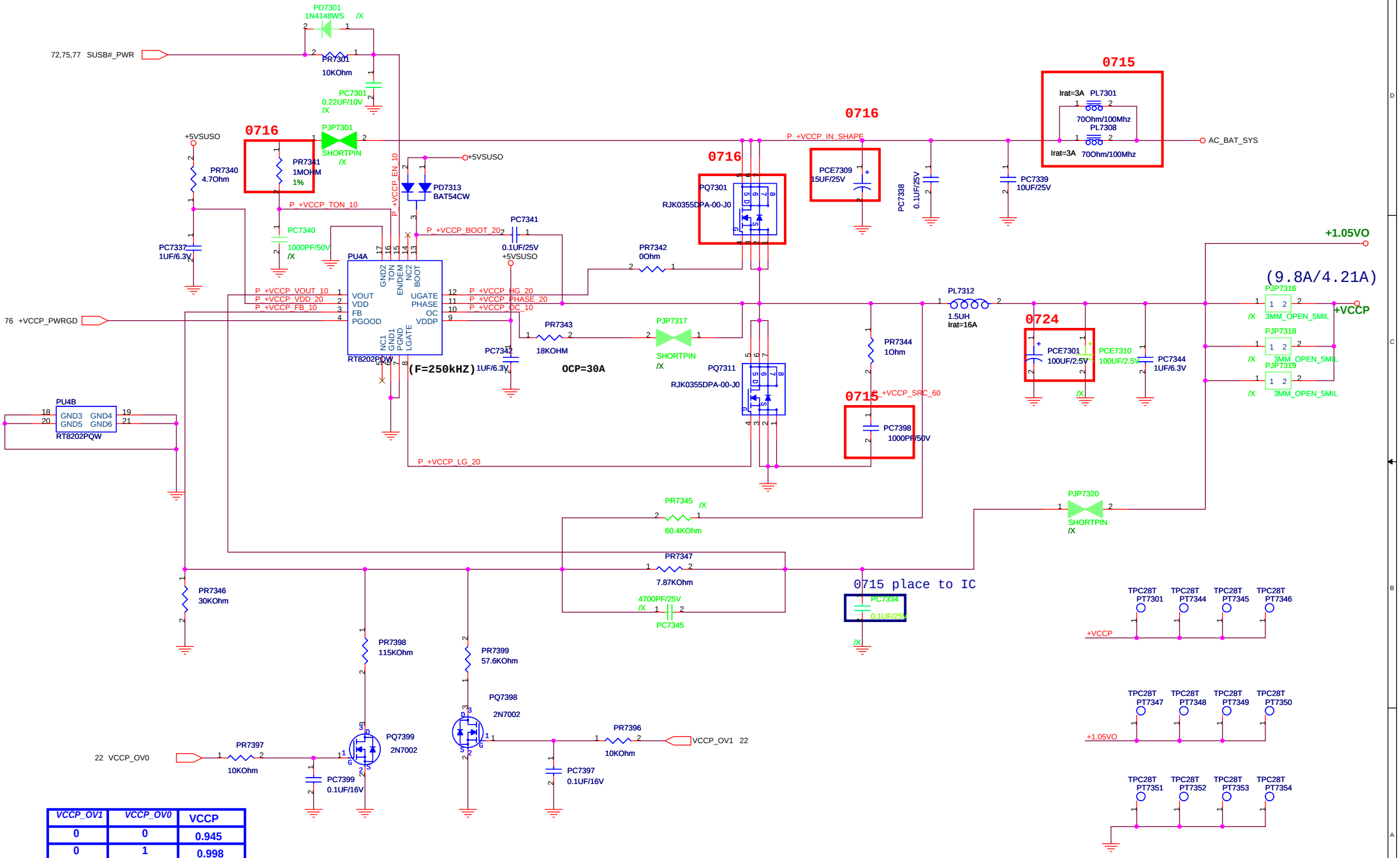

VCCP_OV1	VCCP_OV0	VCCP
0	0	0.945
0	1	0.998
1	0	1.049
1	1	1.1005

<Variant Name>

ASUSTeK COMPUTER INC

Title : Power_+VCCP

Engineer: limy_li

Size	Project Name	Rev
A3	N50A/N51A	1.0

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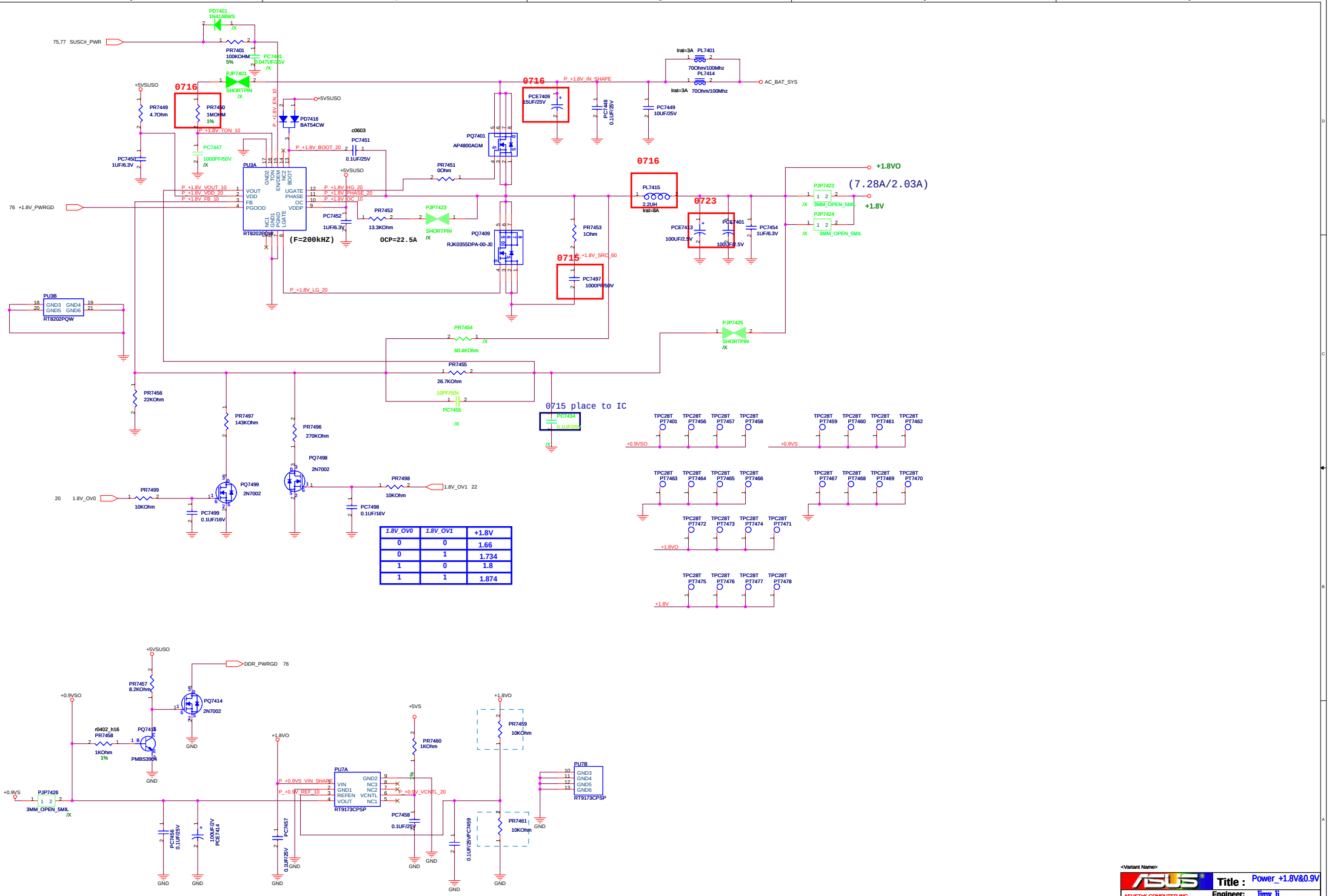

1.8V_OV0	1.8V_OV1	+1.8V
0	0	1.66
0	1	1.734
1	0	1.8
1	1	1.874

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<Variant Name>

ASUSTeK COMPUTER INC

Title : Power_+1.8V&0.9V

Engineer: Jimy_Ji

Size	Project Name	Rev
A2	N50A/N51A	1.0

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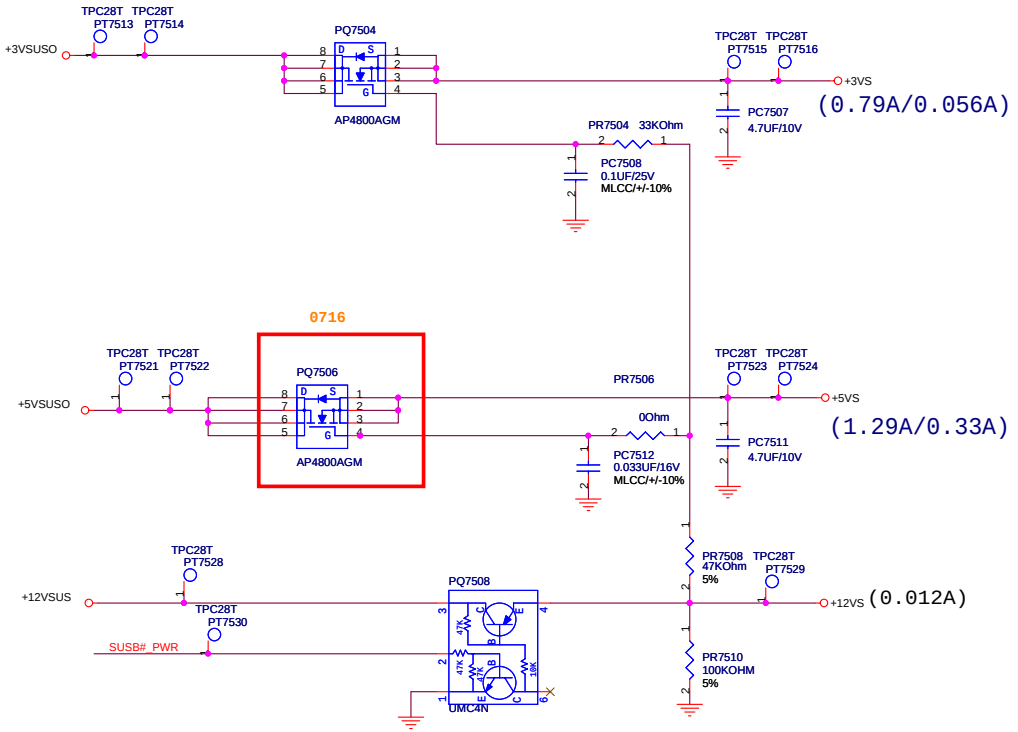
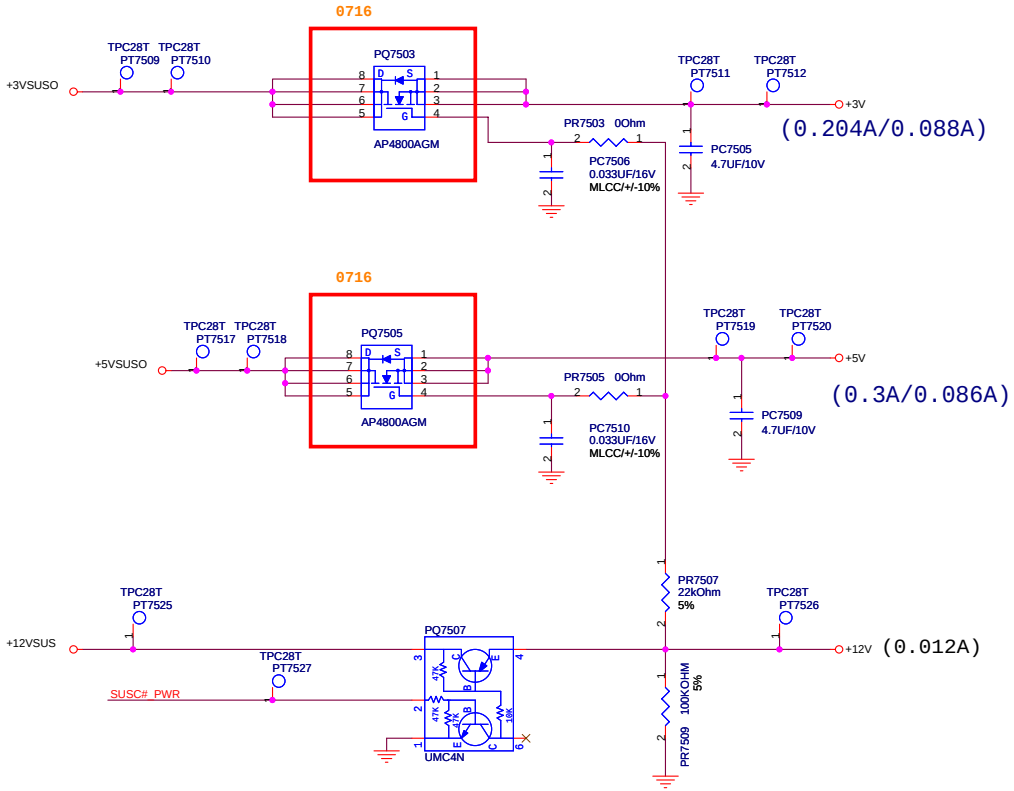
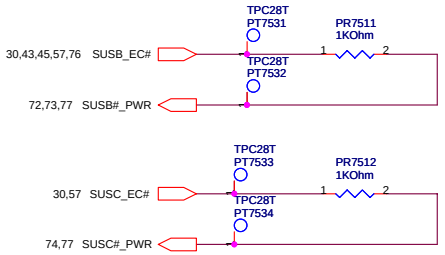
SUSB#_PWR POWER



SUSC#_PWR POWER





<Variant Name>

Title : Power_Load_Switch

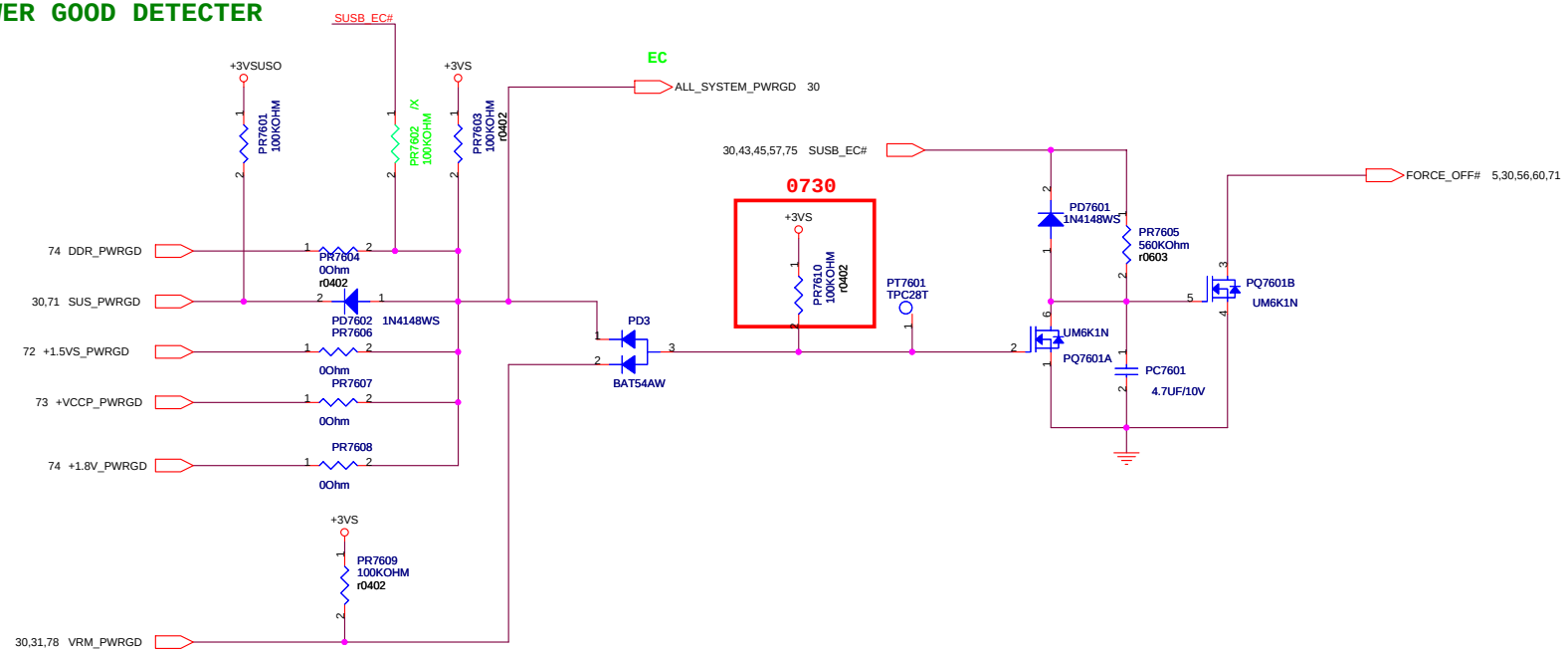
ASUSTeK COMPUTER INC

Engineer: limy_li

Size	Project Name	Rev
Custom	N50A/N51A	1.0

Date: Tuesday, August 05, 2008 Sheet 75 of 79

POWER GOOD DETECTER



<Variant Name>

ASUSTeK COMPUTER INC

Title : Power_good_detecter

Engineer: limy_li

Size	Project Name	Rev
Custom	N50A/N51A	1.0

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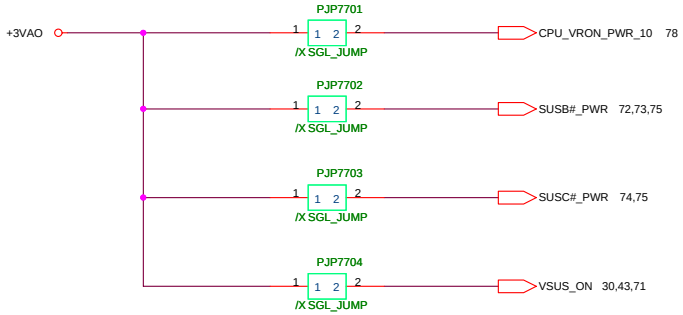

<Variant Name>

ASUSTeK COMPUTER INC

Title : Power_for_test

Engineer: Robin_chen

Size	Project Name	Rev
Custom	N50A/N51A	1.0

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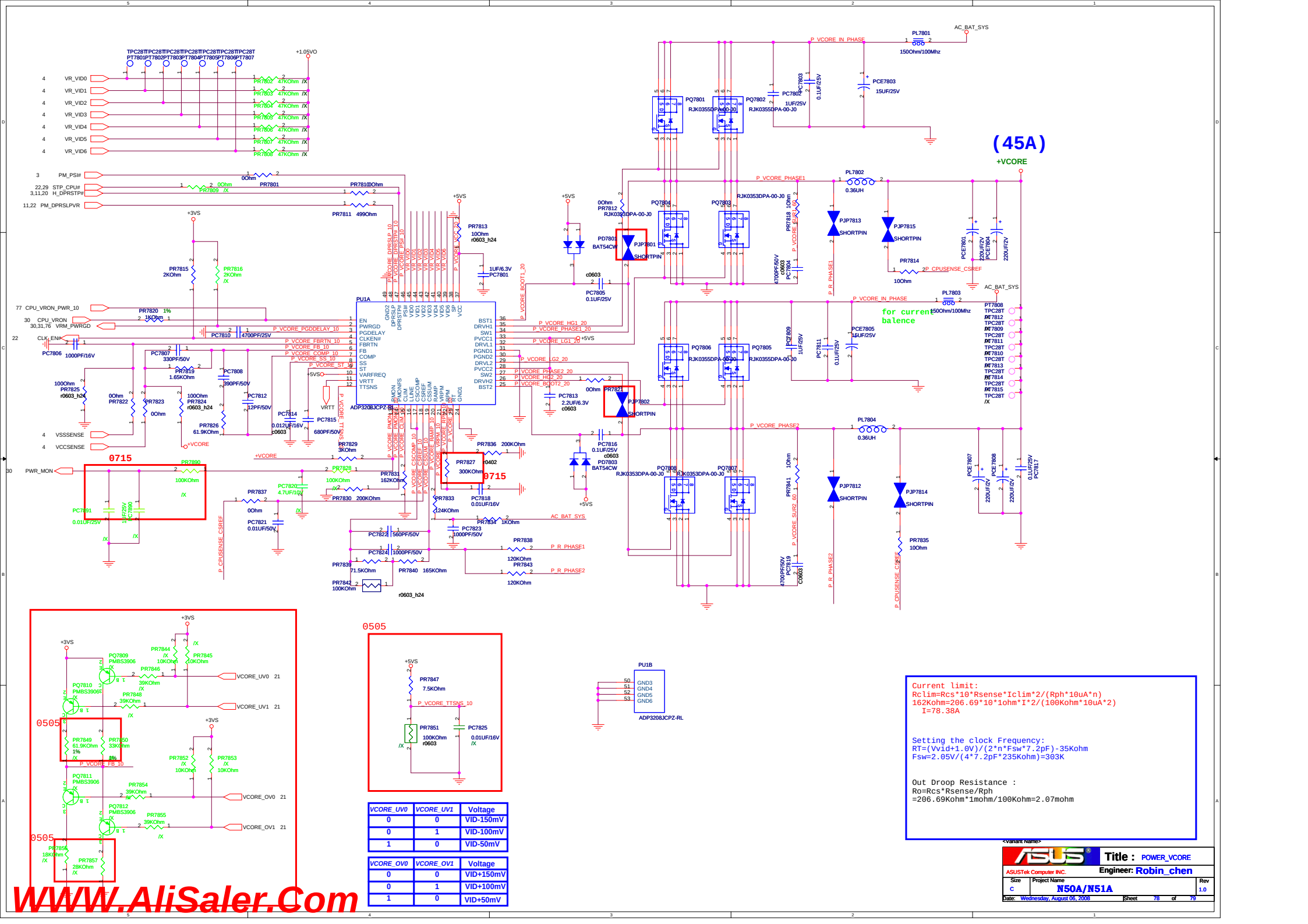

VCORE_UV0	VCORE_UV1	Voltage
0	0	VID-150mV
0	1	VID-100mV
1	0	VID-50mV

VCORE_OV0	VCORE_OV1	Voltage
0	0	VID+150mV
0	1	VID+100mV
1	0	VID+50mV

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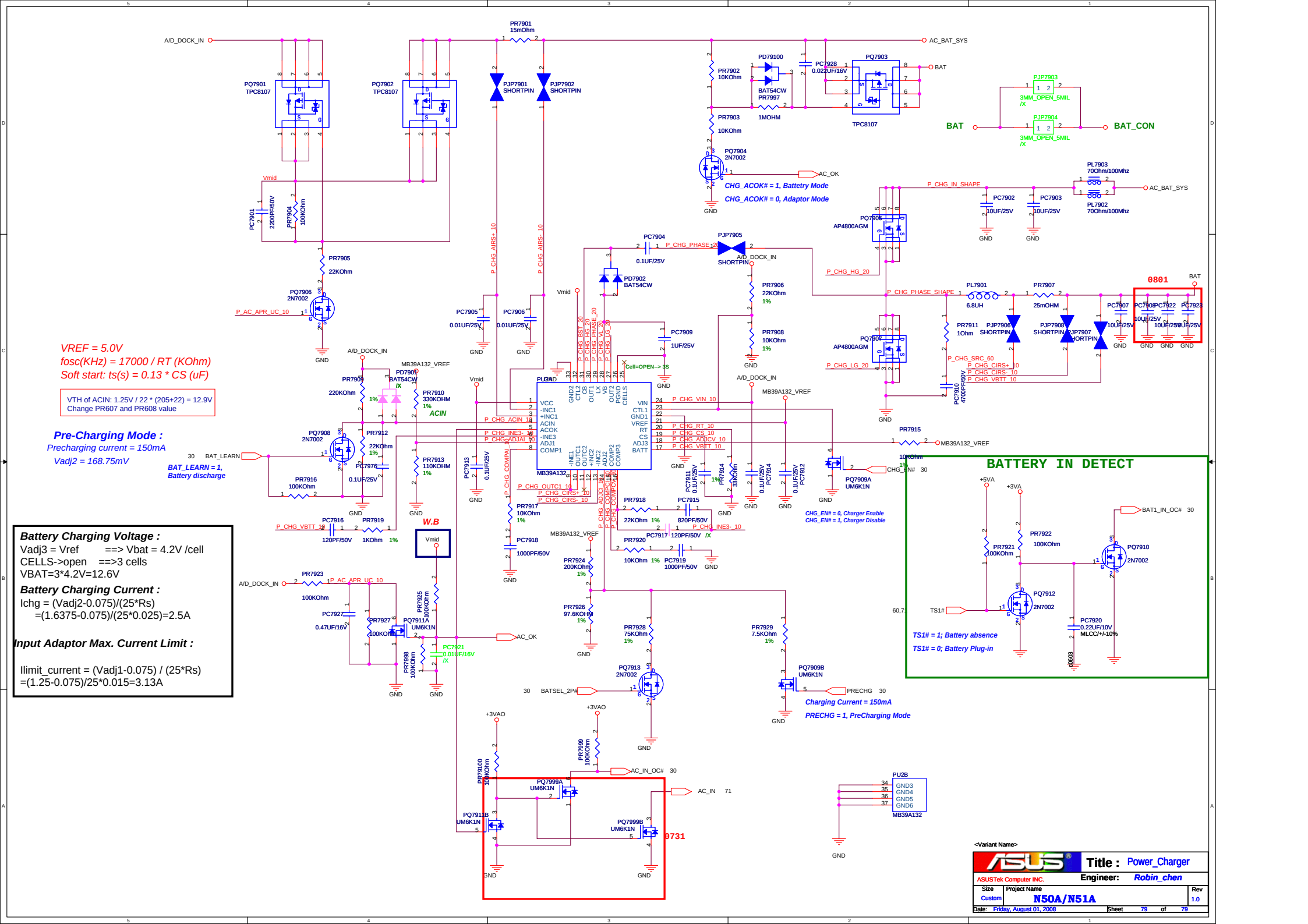
VREF = 5.0V
fosc(KHz) = 17000 / RT (KOhm)
Soft start: ts(s) = 0.13 * CS (uF)
VTH of ACIN: 1.25V / 22 * (205+22) = 12.9V
Change PR607 and PR608 value
Pre-Charging Mode :
Precharging current = 150mA
Vadj2 = 168.75mV
BAT_LEARN = 1, Battery discharge
Battery Charging Voltage :
Vadj3 = Vref ==> Vbat = 4.2V /cell
CELLS->open ==>3 cells
VBAT=3*4.2V=12.6V
Battery Charging Current :
Ichg = (Vadj2-0.075)/(25*Rs)
=(1.6375-0.075)/(25*0.025)=2.5A
Input Adaptor Max. Current Limit :
Ilimit_current = (Vadj1-0.075) / (25*Rs)
=(1.25-0.075)/25*0.015=3.13A
CHG_ACOK# = 1, Battetry Mode
CHG_ACOK# = 0, Adaptor Mode
CHG_EN# = 0, Charger Enable
CHG_EN# = 1, Charger Disable
Charging Current = 150mA
PRECHG = 1, PreCharging Mode
BATTERY IN DETECT
TS1# = 1; Battery absence
TS1# = 0; Battery Plug-in
0801
0731
A/D_DOCK_IN
AC_BAT_SYS
BAT
BAT_CON
AC_OK
MB39A132_VREF
Vmid
W.B
ACIN
Title : Power_Charger
ASUSTek Computer INC.
Engineer: Robin_chen
Project Name N50A/N51A
Rev 1.0
Date: Friday, August 01, 2008
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